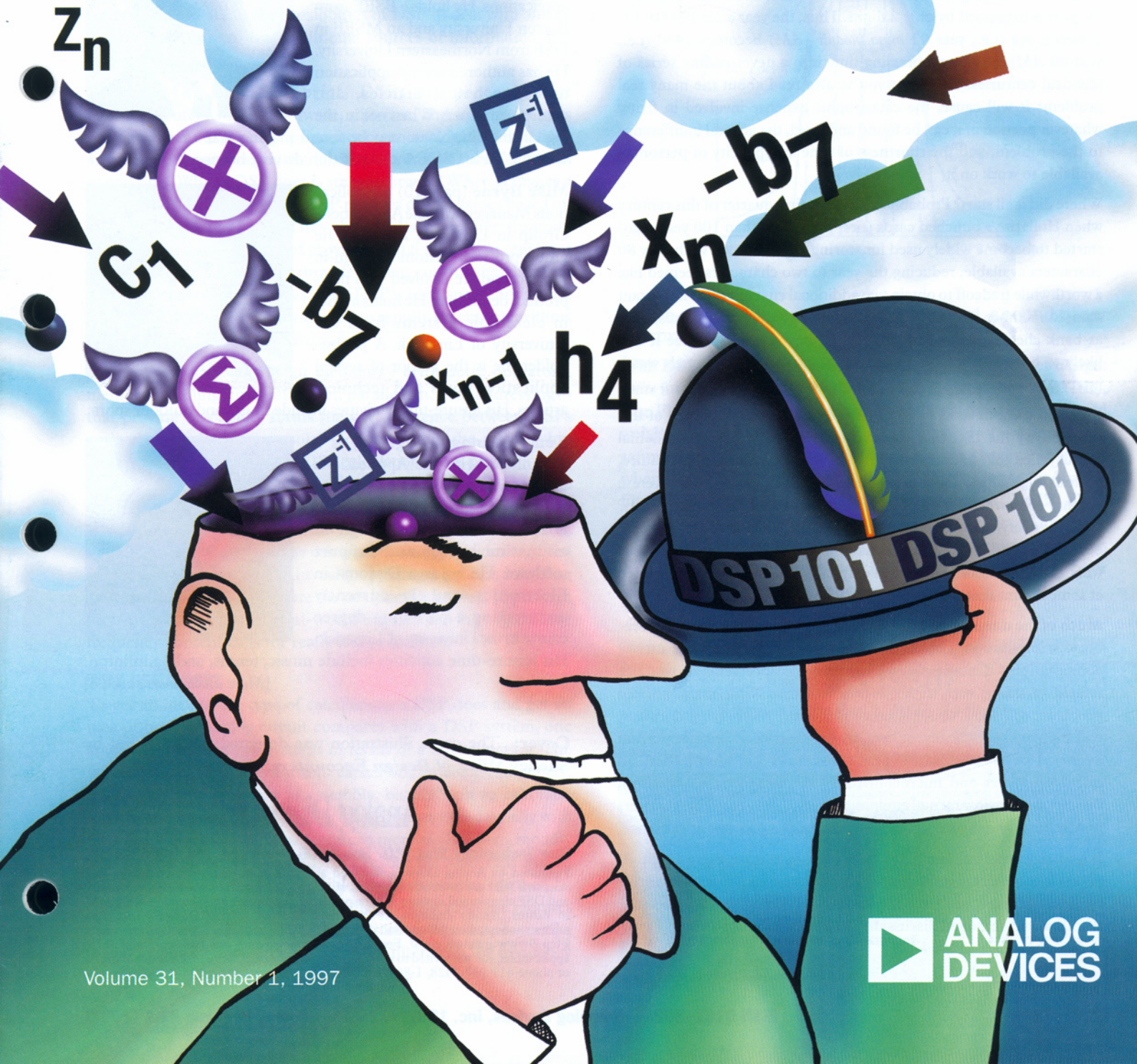
Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 31, Number 1, 1997

ANALOG DEVICES

Editor's Notes

http://www.year2000.com

That's one of the sites where you can read about a major problem we residents of Earth will face as we celebrate the rolling over of the digits after 23:59:59 on December 31, 1999. The problem is that in many cases there aren't enough digits to roll over. Unless something is done about it, many machines and programs will tell you that your age is suddenly $-(100 - y)$, where y is the number of years you've actually lived. If you're 105, you may get a computer letter calling on you to register for kindergarten.

Most of you have probably read about the inability of many computer programs to distinguish between the years 1900 and 2000, because the year is expressed by only 2 digits. Thus, the year after 1999 of the common era (i.e., year 99 *anno moduli—AM*) becomes 1900 (i.e., year 00 *AM*), neatly compressing time into a never-ending series of identical centuries. No doubt you've also read about the many real problems it will cause, the catastrophic expense involved in fixing whatever portion of it can be found and fixed, the general indifference to the problem, and the shortness of time and paucity of personnel available to work on it.

Where did it all start? Probably back in the first quarter of this century when Hollerith's punched cards (first used more than 100 years ago) started to become widely used for storing sortable data. With only 80 characters available, reducing the year to two characters seemed like a worthwhile tradeoff to obtain two additional characters for important data. Remember, this was a time when nearly all printed forms, such as bank checks, had a date line 19__ (they still do!?), since it was likely to be valid throughout one's lifetime (or at least, one's watch interval). Scarcely a thought was given to the next century.

It's interesting to speculate on the role played in the origins of this problem by the fact that the twentieth century is a pre-millenial century, i.e., that to fairly take into account dates far into the future, all four digits have to be allowed to roll over. What if this were a century somewhere in the middle (say, the sixteenth or forty-third)? Then for many, many generations, the maximum century rollover would be a single digit. It's conceivable that more software designers would be willing to take the long view when only a single digit had to be advanced at some distant time within the next 99 years.

Much of the discussion in the popular press has to do with the more-obvious implications, relating to billing and inventory, tax and interest computations, demographics. There are also problems in routines related to safety, such as inspection intervals. While many unfixed problems will show up simultaneously, many more, lying dormant, will show up sporadically, or even by the absence of some important event. Faulty computer programs may lie embedded in microcomputers and microcontrollers in transportation, medical, military, and environmental equipment, perhaps designed by engineers now retired, and manufactured by companies no longer in existence.

It's a hairy problem, one that it behooves us to learn more about. A good place to start is at the above Web address, which is co-sponsored by Peter de Jager, probably the leading consultant on the problem. Another well-reasoned discussion can be found at *http://www.bcs.uk/news/millen/millen.htm#wha*.

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Why Use DSP?

Digital Signal Processing 101—An introductory course in DSP system design: Part 1:

by David Skolnick and Noam Levine

Having heard a lot about digital signal processing (DSP) technology, you may have wanted to find out what can be done with DSP, investigate why DSP is preferred to analog circuitry for many types of operations, and discover how to learn enough to design your own DSP system. This article, the first of a series, is an opportunity to take a substantial first step towards finding answers to your questions. This series is an introduction to DSP topics from the point of view of analog system designers seeking additional tools for handling analog signals. Designers reading this series can learn about the possibilities of DSP to deal with analog signals and where to find additional sources of information and assistance.

What is [a] DSP? In brief, DSPs are processors or microcomputers whose hardware, software, and instruction sets are optimized for high-speed numeric processing applications—an essential for processing digital data representing analog signals in real time. What a DSP does is straightforward. When acting as a digital filter, for example, the DSP receives digital values based on samples of a signal, calculates the results of a filter function operating on these values, and provides digital values that represent the filter output; it can also provide system control signals based on properties of these values. The DSP's high-speed arithmetic and logical hardware is programmed to rapidly execute algorithms modelling the filter transformation.

The combination of design elements—arithmetic operators, memory handling, instruction set, parallelism, data addressing—that provide this ability forms the key difference between DSPs and other kinds of processors. Understanding the relationship between real-time signals and DSP calculation speed provides some background on just how special this combination is. The real-time signal comes to the DSP as a train of individual samples from an analog-to-digital converter (ADC). To do filtering in real-time, the DSP must complete all the calculations and operations required for processing each sample (usually updating a process involving many previous samples) before the next sample arrives. To perform high-order filtering of real-world signals having significant frequency content calls for really fast processors.

WHY USE A DSP?

To get an idea of the type of calculations a DSP does and get an idea of how an analog circuit compares with a DSP system, one could compare the two systems in terms of a filter function. The familiar analog filter uses resistors, capacitors, inductors, amplifiers. It can be cheap and easy to assemble, but difficult to calibrate, modify, and maintain—a difficulty that increases exponentially with filter order. For many purposes, one can more easily design, modify, and depend on filters using a DSP because the filter function on the DSP is software-based, flexible, and repeatable. Further, to create flexibly adjustable filters with higher-order response requires only software modifications, with no additional hardware—unlike purely analog circuits. An ideal bandpass filter, with the frequency response shown in Figure 1, would have the following characteristics:

- a response within the passband that is completely flat with zero phase shift
- infinite attenuation in the stopband.

Useful additions would include:

- passband tuning and width control
- stopband rolloff control.

As Figure 1 shows, an analog approach using second-order filters would require quite a few staggered high-Q sections; the difficulty of tuning and adjusting it can be imagined.

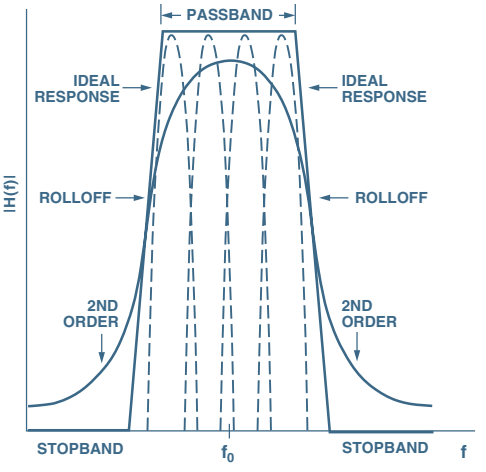

Figure 1. An ideal bandpass filter and second-order approximations.

With DSP software, there are two basic approaches to filter design: *finite* impulse response (FIR) and *infinite* impulse response (IIR). The FIR filter's time response to an impulse is the straightforward weighted sum of the present and a *finite* number of previous input samples. Having no feedback, its response to a given sample ends when the sample reaches the "end of the line" (Figure 2). An FIR filter's frequency response has no poles, only zeros. The IIR filter, by comparison, is called infinite because it is a recursive function: its output is a weighted sum of inputs *and* outputs. Since it is recursive, its response can continue indefinitely. An IIR filter frequency response has both poles and zeros.

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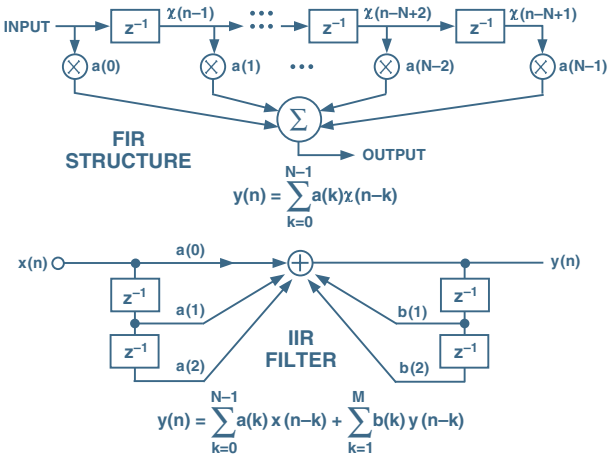

Figure 2. Filter equations and delay-line representation.

The *x*s are the input samples, *y*s are the output samples, *a*s are input sample weightings, and *b*s are output sample weightings. *n* is the present sample time, and *M* and *N* are the number of samples programmed (the filter's *order*). Note that the arithmetic operations indicated for both types are simply sums and products—in potentially great number. In fact, multiply-and-add is the case for many DSP algorithms that represent mathematical operations of great sophistication and complexity.

Approximating an ideal filter consists of applying a transfer function with appropriate coefficients and a high enough order, or number of *taps* (considering the train of input samples as a tapped delay line). Figure 3 shows the response of a 90-tap FIR filter compared with sharp-cutoff Chebyshev filters of various orders. The 90-tap example suggests how close the filter can come to approximating an ideal filter. Within a DSP system, programming a 90-tap FIR filter—like the one in Figure 3—is not a difficult task. By comparison, it would not be cost-effective to attempt this level of approximation with a purely analog circuit. Another crucial point in favor of using a DSP to approximate the ideal filter is long-term stability. With an FIR (or an IIR having sufficient resolution to avoid truncation-error buildup), the programmable DSP achieves the same response, time after time. Purely analog filter responses of high order are less stable with time.

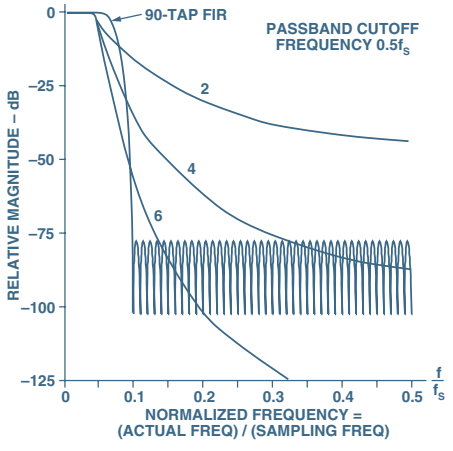

Figure 3. 90-tap FIR filter response compared with those of sharp cutoff Chebyshev filters.

Mathematical transform theory and practice are the core requirement for creating DSP applications and understanding their limits. This article series walks through a few signal-analysis and -processing examples to introduce DSP concepts. The series also provides references to texts for further study and identifies software tools that ease the development of signal-processing software.

SAMPLING REAL-WORLD SIGNALS

Real-world phenomena are analog—the continuously changing energy levels of physical processes like sound, light, heat, electricity, magnetism. A transducer converts these levels into manageable electrical voltage and current *signals*, and an ADC samples and converts these signals to digital for processing. The conversion rate, or sampling frequency, of the ADC is critically important in digital processing of real-world signals.

This sampling rate is determined by the amount of signal information that is needed for processing the signals adequately for a given application. In order for an ADC to provide enough samples to accurately describe the real-world signal, the sampling rate must be at least twice the highest-frequency component of the analog signal. For example, to accurately describe an audio signal containing frequencies up to 20 kHz, the ADC must sample the signal at a minimum of 40 kHz. Since arriving signals can easily contain component frequencies above 20 kHz (including noise), they must be removed before sampling by feeding the signal through a low-pass filter ahead of the ADC. This filter, known as an *anti-aliasing* filter, is intended to remove the frequencies above 20 kHz that could corrupt the converted signal.

However, the anti-aliasing filter has a finite frequency rolloff, so additional bandwidth must be provided for the filter's transition band. For example, with an input signal bandwidth of 20 kHz, one might allow 2 to 4 kHz of extra bandwidth.

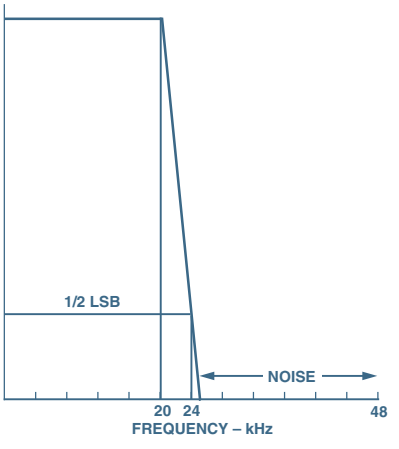

Figure 4. Antialiasing filter ideal response.

Figure 4 depicts the filter needed to reject any signals with frequencies above half of a 48-kHz sampling rate. *Rejection* means attenuation to less than 1/2 least-significant bit (LSB) of the ADC's resolution. One way to achieve this level of rejection without a highly sophisticated analog filter is to use an *oversampling* converter, such as a sigma-delta ADC. It typically obtains low-resolution (e.g., 1-bit) samples at megahertz rates—much faster than twice the highest frequency component—greatly easing the requirement for the analog filter ahead of the converter. An internal digital filter (DSP at work!) restores the required resolution and frequency response. For many applications, oversampling converters reduce system design effort and cost.

PROCESSING REAL-WORLD SIGNALS

The ADC sampling rate depends on the bandwidth of the analog signal being sampled. This sampling rate sets the pace at which samples are available for processing. Once the system bandwidth requirements have established the A/D converter sampling rate, the designer can begin to explore the speed requirements of the DSP processor.

Processing speed at a required sample rate is influenced by algorithm complexity. As a rule, the DSP needs to finish all operations relating to the first sample before receiving the second sample. The time between samples is the time budget for the DSP to perform all processing tasks. For the audio example, a 48-kHz sampling rate corresponds to a 20.833-µs sampling interval. Figure 5 relates the analog signal and digital sampling rate.

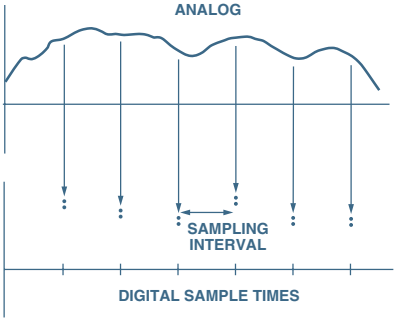

Figure 5. Sampling train and processing time.

Next consider the relation between the speed of the DSP and complexity of the algorithm (the software containing the transform or other set of numeric operations). Complex algorithms require more processing tasks. Because the time between samples is fixed, the higher complexity calls for faster processing.

For example, suppose that the algorithm requires 50 processing operations to be performed between samples. Using the previous example's 48-kHz sampling rate (20.833-µs sampling interval), one can calculate the minimum required DSP processor speed, in millions of operations per second (MOPS) as follows:

$$DSP\ Speed = \frac{Operations}{Sampling\ Interval} = \frac{50}{20.833\ \mu s} = 2.4\ \text{MOPS}$$

Thus if all of the time between samples is available for operations to implement the algorithm, a processor with a performance level of 2.4 MOPS is required. Note that the two common ratings for DSPs, based on *operations* per second (MOPS) and *instructions* per second (MIPS), are not the same. A processor with a 10-MIPS rating that can perform 8 operations per instruction has basically the same performance as a faster processor with a 40 MIPS rating that can only perform 2 operations per instruction.

SAMPLING VARIOUS REAL-WORLD SIGNALS

There are two basic ways to acquire data, either one sample at a time or one frame at a time (continuous processing vs. batch processing). Sample-based systems, like a digital filter, acquire data one sample at a time. As shown in Figure 6, at each tick of the clock, a sample comes into the system and a processed sample is output. The output waveform develops continuously.

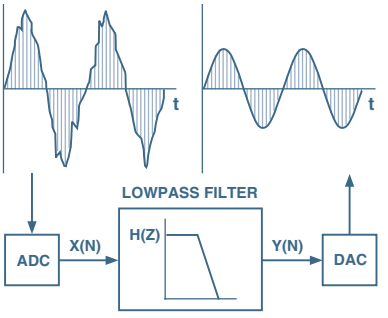

Figure 6. Example of continuous processing of samples in digital filter.

Frame-based systems, like a spectrum analyzer, which determines the frequency components of a time-varying waveform, acquire a frame (or block of samples). Processing occurs on the entire frame of data and results in a frame of transformed data, as shown in Figure 7.

Figure 7. Example of batch processing of a block of data.

For an audio sampling rate of 48 kHz, a processor working on a frame of 1024 samples has a frame acquisition interval of 21.33 ms (i.e., 1024 × 20.833 µs = 21.33 ms). Here the DSP has 21.33 ms to complete all the required processing tasks for that frame of data. If the system handles signals in real time, it must not lose any data; so while the DSP is processing the first frame, it must also be acquiring the second frame. Acquiring the data is one area where special architectural features of DSPs come into play: Seamless data acquisition is facilitated by a processor's flexible data-addressing capabilities in conjunction with its direct memory-accessing (DMA) channels.

RESPONDING TO REAL-WORLD SIGNALS

One cannot assume that all the time between samples is available for the execution of processing instructions. In reality, time must be budgeted for the processor to respond to external devices, controlling the flow of data in and out. Typically, an external device (such as an ADC) signals the processor using an interrupt. The DSP's response time to that interrupt, or *interrupt latency*, directly influences how much time remains for actual signal processing.

Interrupt latency (response delay) depends on several factors; the most dominant is the DSP architecture's instruction pipelining. An instruction pipeline consists of the number of instruction cycles that occur between the time an interrupt is received and the time that program execution resumes. More pipeline levels in a DSP result in longer interrupt latency. For example, if a processor has a 20-ns cycle time and requires 10 cycles to respond to an interrupt, 200 ns elapse before it executes any signal-processing instructions.

When data is acquired one sample at a time, this 200-ns overhead will not hurt if the DSP finishes the processing of each sample before the next arrives. When data is acquired sample-by-sample while processing a frame at a time, however, an interrupted system wastes processor instruction cycles. For example, a system with a

200-ns interrupt response time running a frame-based algorithm, such as the FFT, with a frame size of 1024 samples, would require 204.8 µs of overhead. That amounts to more than 10,000 instruction cycles wasted to latency—productive time when the DSP could be performing signal processing. This waste is easy to avoid in DSPs having architectural features such as DMA and dual memory access; they let the DSP receive and store data without interrupting the processor.

DEVELOPING A DSP SYSTEM

Having discussed the role of the processor, the ADC, the anti-aliasing filter, and the timing relationships between these components, it is time to look at a complete DSP system. Figure 8 shows the building blocks of a typical DSP system that could be used for data acquisition and control.

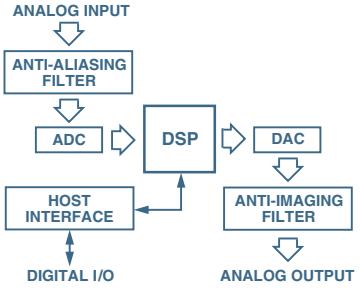

Figure 8. Putting together elements of a DSP system.

Note how few components make up the DSP system, because so much of the system's functionality comes from the programmable DSP. Converters funnel data into and out of the DSP; the ADC timing is controlled by a precise sampling clock. To simplify system design, many converter devices available today combine some or all of the following: an A/D converter, a D/A converter, a sampling clock, and filters for anti-aliasing and anti-imaging. The clock oscillator in these types of I/O components is separately controlled by an external crystal. Here are some important points about the data flow in this sort of DSP system:

Analog Input: The analog signal is appropriately band-limited by the anti-aliasing filter and applied to the input of the ADC. At the selected sampling time, the converter interrupts the DSP processor and makes the digital sample available. The choice between serial and parallel interfacing between the ADC and DSP depends on the amount of data, design complexity trade-offs, space, power, and price.

Digital Signal Processing: The incoming data is handled by the DSP's algorithm software. When the processor completes the required calculations, it sends the result to the DAC. Because the signal processing is programmable, considerable flexibility is available in handling the data and improving system performance with incremental programming adjustments.

Analog Output: The DAC converts the DSP's output into the desired analog output at the next sample clock. The converter's output is smoothed by a low-pass, *anti-imaging* filter (also called a reconstruction filter), to produce the reconstructed analog signal.

Host Interface: An optional host interface lets the DSP communicate with external systems, sending and receiving data and control information.

REVIEW AND PREVIEW

The goal of this article has been to provide an overview of major DSP design concepts and explain some of the reasons why a DSP is better suited that analog circuitry for some applications. The issues introduced in this article include:

- DSP overview
- Real-time DSP operation
- Real-world signals
- Sampling rates and anti-alias filtering
- DSP algorithm time budget
- Sample driven versus frame driven data acquisition

Because these issues involve many valuable levels of detail that we could not do justice to in this brief article, you should consider reading Richard Higgins's text, *Digital Signal Processing in VLSI* (see References below). This text provides a complete overview of DSP theory, implementation issues, and reduction to practice (with devices available at the time it was published), plus exercises and examples. The Reference section below also contains other sources that further amplify this article's issues. To prepare for the next articles in this series, you might want to get free copies of the *ADSP-2100 Family User's Manual** and the *ADSP-2106x SHARC User's Manual*.* These texts provide information on Analog Devices's fixed- and floating-point DSP architectures, a major topic in these articles. The next article will cover the following territory:

• **Mathematical overview of signal processing:** It will present the mathematics for the transform functions (frequency domain) and convolution functions (time domain) that appear throughout the series. While the mathematical treatment is necessarily incomplete (no derivations), there will be sufficient detail for considering how to program the operations.

• **DSP architecture:** The article will discuss the nature and functioning of the DSP's arithmetic-logic unit (ALU), multiply-accumulator (MAC), barrel-shifter, and memory busses—and describe the numeric operations that support DSP functions.

• **DSP programming concepts:** A discussion of programming will bring together theory and practice (math and architecture). Finally, it will lay out the main parameters for a series-length DSP design project, provided as an example.

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Selecting Mixed Signal Components for Digital Communication Systems—II: Sharing the Channel

by Dave Robertson

Part I provided an introduction to the concept of channel capacity—and its dependence on bandwidth and SNR; Part II gave a brief summary of different types of modulation schemes. This segment discusses communications signal-processing issues that arise when multiple users share the same transmission medium .

SHARING THE CHANNEL

Selection of an appropriate modulation scheme is only part of the problem of defining a communications network. In most cases, the transmission medium must accommodate signals from more than a single transmitter. The most obvious case of such multiple use is the airwaves; they must carry a variety of wireless traffic, from broadcast radio and television, to cellular telephony, to CB and short-wave radio. Even a simple twisted-pair telephone wire, which represents a dedicated line between the phone company central office and a user, must carry both incoming and outgoing voice and data during a call.

In most cases, the key to effective multiplexing of independent transmissions is proper observance of "live and let live" protocols, enabling the effective transmission of the desired message without undue interference to other transmissions. There are a variety of approaches towards sharing a communications medium among multiple users; each has its own requirements affecting component selection. Most of these schemes are usable for both analog and digital communications; but the flexibility of time compression, and other features available in digital communications, opens up more options.

TDMA—time-division multiple access: perhaps the most obvious way of sharing the communications channel is to "take turns": only one transmitter at a time is allocated the channel. There must of course be some sort of protocol to establish who has the transmission privilege, when, how often, and for how long. A simple example is the walkie-talkie user's employment of the word "over" to indicate the termination of a transmission stream and freeing up the communications channel for other users to transmit.

A more formal arrangement is usually desirable, especially when each user is to be allotted a very brief—but repetitive—participation. An overall time period can be divided into designated "slots", with each of the transmitters assigned a different time slot for transmission (Figure 1). This kind of scheme requires synchronization of all the transmitters, plus a "supervisor" to assign time slots as new transmitters want to enter the channel—and to keep track of slots vacated. Some "overhead" space must be provided to allow for transitions between transmitter time slots; the better the synchronization, the less time lost to these transition periods. Time multiplexing also means that the stream of data from a given transmitter is not continuous, but in bursts. To represent a continuous conversation (say in a cellular phone call), the digitized information acquired during the period between transmissions must be time compressed, transmitted in a short burst, then expanded in the receiver to form a transparently continuous message.

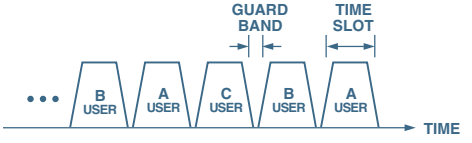


Figure 1. Illustration of time multiplexing, showing guard bands.

The analogy of a panel discussion is sometimes used to illustrate the nature of TDMA. A participant who interrupts out of turn or rattles on and on endlessly commits "violations of the TDMA protocol." The European GSM digital cellular telephony standard makes use of TDMA; each channel carries eight phone calls simultaneously in a repeated transmitting sequence of eight time slots.

Component selection for TDMA systems must involve careful consideration of bandwidths and settling times; long time constants of components with insufficient bandwidth will tend to cause signals to "bleed into" an adjacent user's time slot.

FDMA—frequency-division multiple access: anyone who receives TV or radio broadcasts at home is familiar with an example of frequency-division multiple access. In this case, multiple transmitters can simultaneously transmit without interference (at a given power level in a given geographical area) by keeping each frequency in their transmissions within a designated frequency slot. The receiver determines which channel is to be recovered by tuning to the desired frequency slot. It is important that each transmitter's frequency limits be strictly observed; any transgressions would create interference in the neighboring channels. (Figure 2)

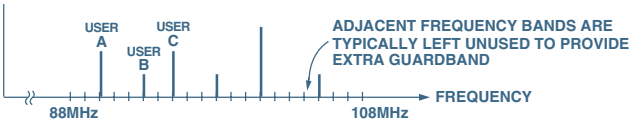


Figure 2. Illustration of frequency multiplexing, showing unused frequency bands to provide separation.

Using the conversational analogy, this might be like providing a set of booths, one for each speaker; if they speak quietly enough, all "transmitters" can broadcast simultaneously, and a listener may "tune in" by listening at the desired booth.

Almost all wireless applications are subject to frequency band constraints; national and international regulatory bodies, e.g., the FCC in the United States, license the transmitter to specific frequencies or restrict its class to specific bands. Wired applications like cable TV also use frequency separation to allow simultaneous transmission of hundreds of channels (both analog and digital).

Keeping within the specified frequency constraints has numerous ramifications for component selection. For example, some component in the system will be used as a precise frequency reference. It could be an absolute frequency reference, like a crystal,

or it might contain a circuit that receives and "locks on" to an external reference frequency. Components in the transmission path must have carefully limited spectral content; this can be done through filtering—but it is also necessary to control component linearity, so as not to generate incidental "out of band" harmonics and other spurious frequency components.

CDMA—Carrier Division Multiple Access—Continuing the conversation analogies, suppose that 10 people are trying to carry on 5 simultaneous one-on-one conversations in a small room. Suppose further that one pair agrees to converse in English, another in French, the others in Chinese, Finnish, and Arabic—and all are monolingual. If you were a member of the English speaking pair, you would hear a din of background "babble", but the only intelligible information would be in English. So it's easy to see that all 5 conversations could take place simultaneously in the same room (though in practice, everyone would probably get a headache).

This is essentially a description of the underlying idea of carrier division multiple access. All users transmit and receive over the same frequency band, but each pair is assigned a unique code sequence. The digital bit stream you wish to send is modulated with this unique code sequence and transmitted. A receiver will receive the combined modulated bit streams of all the transmitters. If the receiver demodulates this composite signal with the same unique code, it essentially performs a cross-correlation operation: the bit stream that was modulated with the same code sequence will be recovered; all the other transmitted signals that were modulated with different codes will be rejected as "noise".

Modulation with the special code tends to spread the spectrum of the initial digital bit stream over a much wider bandwidth, which helps improve its immunity from interference. Despite this spectral spreading, spectral efficiency can be maintained, because multiple users can share the same bandwidth. Adding more users simply leads to the appearance of increased noise in the channel

Examples of CDMA systems include the IS95 Digital Cellular standard in the US and numerous military "spread spectrum" communications applications (an additional advantage of modulating the transmitted signal with a unique signal is that it is essentially encrypted; a receiver cannot recover the transmitted message without the unique modulation sequence). Though CDMA systems involve greater digital complexity, the performance requirements for their analog components are reduced. However, because multiple transmitters will be broadcasting in the same channel at the same time, it is usually desirable to minimize the contributions to background and spurious noise by transmitter components.

SDMA—Space Division Multiple Access: Returning to the conversation analogy, another way to carry on simultaneous one-on-one conversations in the same room is to move to opposite corners of the room and speak in relatively hushed tones. This captures the spirit of SDMA. In wireless applications, signal strength falls off rapidly with increasing distance from the transmitting antenna. At a great enough distance, the signal can be considered to have faded completely, from which point a new transmitter could reuse the same frequency or time slot for a different signal (Figure 3). In broadcast radio, the same frequency can be reused in different cities, provided that they are far enough apart.*

*The attenuation of signal with distance is a strong function of frequency: The higher the transmitter frequency, the faster the rolloff.

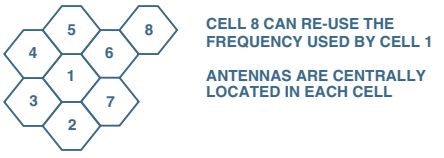


Figure 3. Illustration of geographical multiplexing, showing honeycomb of cells with base-station antennas at centers.

The concept of channel re-use with distance underlies the term "cellular telephony." Cell size is determined by the area of effective coverage by a given transmitter, and the same frequencies can be reused in other cells. In practice, however, patterns are designed so that adjacent cells will not re-use the same frequencies. Conventional antennas radiate in all directions, producing a circular coverage area and the "honeycomb" cellular pattern in Figure 3. Modern technology has added new dimensions to the concept of SDMA with the development of focused, or beam steering antennas. Phased-array technology can create a focused, directional signal transmission pattern aimed at either an individual target receiver or a particular target area (e.g., a specific highway at rush hour). This can allow more rapid re-use of frequency spectrum, thereby effectively increasing total capacity for wireless applications.

Advanced digital communications systems use combinations of these multiplexing schemes to effectively pack as much capacity as possible into the available transmission channel. For example, GSM cellular phones use TDMA, FDMA and SDMA to allocate traffic. Even many wired applications make use of TDMA and FDMA protocols. Although these multiplexing arrangements typically add to the system complexity, the effective increase in channel capacity more than offsets increases in component cost.

THE NEAR/FAR PROBLEM

In previous installments, we have discussed the impact of error rate and modulation scheme on the required dynamic range in a digital communications system. However, in many applications, the *multiplexing* arrangements create the ultimate demands on dynamic range in the communications receiver.

In any application, the strength of the received signal is a function of the strength of the transmitted signal, the distance from the transmitter, and numerous environmental factors relating to the transmission medium (be it wireless or wired). Most communications systems are designed to work over a variety of distances, and so have to be designed to accommodate a large variation in power of the received signal.

Consider, for example, a cellular telephony application. The receiver circuitry must be designed to recover the weak signal resulting from a transmission while at the very edge of the "cell". This capability to recover weak signals is often referred to as a receiver's *sensitivity*. To recover such weak signals, it seems appropriate to include gain stages in the receive circuitry. Consistent with good, low-noise design practice, one might expect to put the gain as early in the signal path as possible to quickly boost the signal above the noise floor of subsequent stages.

Unfortunately, this same receiver must also be capable of receiving the signal transmitted by a user standing directly under the base station's antenna. In the case of GSM, for example, this signal can be up to 90 dB stronger than the weakest signal. If the receiver

has too much gain in the signal path, the strong signal can saturate the gain stages. For modulation schemes that include amplitude information (including AM and QAM), this will essentially destroy the signal. Phase and frequency modulation approaches may be more tolerant of this clipping, depending on the circumstances. (The clipping will still create distortion products which are sufficient to cause problems, even in phase-modulation schemes.)

A basic approach to addressing the near/far dynamic range problem is to use variable/programmable gain stages in the receive signal path. Automatic gain control (AGC) allows the gain to be adjusted in response to the strength of the received signal. An important design consideration, though, is how rapidly the gain needs to be adjusted. For example, in ADSL (asymmetric digital subscriber line—see sidebar) modems, the received signal strength changes as outdoor temperature changes affect the line impedance, so time constants of minutes would be tolerable. On the other hand cellular phone receivers must be designed to track the signals from fast moving vehicles that may be moving into or emerging from the shadows of buildings or other signal obstacles, so very rapid gain changes are required. TDMA systems put an additional demand on gain-ranging circuitry, because the near/far signals could be located in adjacent TDMA time slots; in this case, the circuitry would have to change gains and settle in the transition period between time slots.

FDMA systems offer a different kind of near/far challenge. Here, the worst case to consider is recovery of a weak signal in a frequency slot next to strong signal (Figure 4). Since both signals are present simultaneously as a composite at the input of a gain stage, the gain is set according to the level of the stronger signal; the weak signal could be lost in the noise floor (in this case, the noise floor could be thermal noise or quantization noise of an A/D converter.)

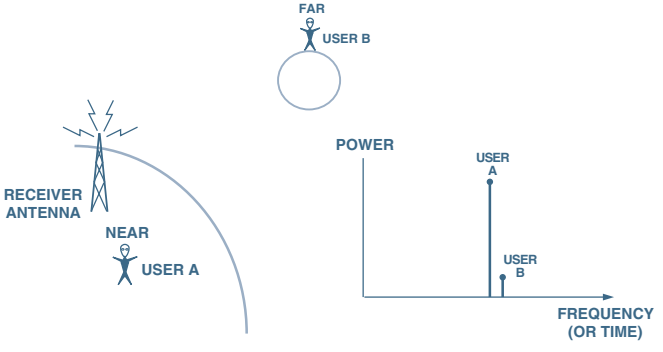


Figure 4. Near-far effect calls for the ability to handle wide dynamic range between adjacent channels.

Even if subsequent stages have a low enough noise floor to provide dynamic range to recover the weak signal, there must also be a very stringent constraint on the dynamic linearity of the gain stage; harmonics or other spurious responses of the strong signal that wind up in the wrong frequency bin could easily obliterate the weaker desired signal. To reduce this interference problem, most FDMA systems attempt to filter out unwanted signals early in the receive circuitry. The ability to discriminate against unwanted signals in adjacent frequency bands is usually referred to as a receiver's *selectivity*.

Most radio designs feature a cascaded series of filters and gain stages (some of which may be variable) to remove/attenuate strong interferers, then amplify the desired signal to a level that can be readily demodulated. Wideband radios, however, attempt to simultaneously recover all the signals in one receiver; they cannot use analog discrimination filters; accordingly, wideband receivers typically have the most stringent requirements on dynamic range in their analog circuitry and converters. Interestingly enough, even applications where you think you have the communications channel to yourself can suffer from simultaneous near/far signals. For example, in ADSL modems, the system must be designed for the scenario where the near-end echo (leakage from the local transmitter) appears as an interfering signal that is actually up to 60 dB stronger than the desired receive signal.

In CDMA systems the near/far problem is a little more difficult to describe. Since all signals are simultaneously transmitted in the same frequency space, filtering cannot be used to discriminate against unwanted signals (though it is still used to eliminate signals in adjacent bands). CDMA employs demodulation using a carrier unique to the desired signal to extract the desired from the unwanted signals; signals modulated with a different carrier appear as background noise. The ability to successfully recover the signal is set by the total noise energy—including that of the other carriers—in the band. Since filtering can't be used to discriminate, the best situation to strive for is to have all signals arrive at the base-station antenna at equal power. To achieve this, many CDMA systems communicate the received power levels back to the transmitters so that power of the individual signal components may be adjusted to equalize power levels at the base-station receiver. To help reduce their near/far problem, TDMA systems could also use this kind of power control, though it tends to require a more-sophisticated (i.e., costly) handset.

ASYMMETRIC DIGITAL SUBSCRIBER LINE

ADSL is one of the many technologies competing to bring broadband digital services into the home. The concept underlying ADSL is to take advantage of the twisted-pair wires that already provide almost universal telephone service to homes in the United States. Other services providing a two-way flow of information, such as ISDN (integrated services digital network), require an additional, dedicated wire to provide service.

ADSL uses frequency-division multiplexing (FDM) to convey modulated digital information in the frequency space between 20 kHz and 1.2 MHz, above the frequency space occupied by conventional voice traffic. This frequency separation allows an ADSL modem to operate without disturbing a phone call occurring at the same time—an extremely important feature.

The ANSI standard for ADSL provides for simultaneous upstream (outgoing from the home) and downstream (incoming to the home) transmission using either FDM (separating the upstream and downstream signals in frequency) or echo cancelling. Echo cancelling uses sophisticated signal processing (analog, digital, or both) to separate the strong transmitted signal from the weaker received signal, passing only the received signal to the demodulator. Using the conversational model, this is analogous to a person who can effectively talk and listen at the same time.

Controller Board System Allows For Easy Evaluation Of General-Purpose Converters

by Mike Byrne & Ken Kavanagh

A critical task when designing a system using an analog-to-digital converter is the actual choice of the converter to be used. Constraints such as power, price, and size—along with system requirements of resolution and performance parameters will narrow the choice. However, the designer may still be left with a number of converters which at first glance will perform in the application. One option is to simply to choose a converter based on data-sheet information; but the prudent engineer will actually want to see how the part performs under the conditions required by the application. At issue, though, is how to spend as little time as possible on the evaluation, since much of it will be spent evaluating converters that will be eliminated from consideration.

Evaluating converters is not an easy task. Hardware design work and careful PCB layout are required to allow the part to achieve its specified analog performance. Even if the hardware problem is solved by use of a standard evaluation board, software routines will be required to control the part and read back the data. In today's diverse market, the wide variety of available converters, especially those from different manufacturers, are housed in proprietary pinouts and generally require different software routines for control and access.

Given this background, any tools that enable the designer to evaluate the converter more easily are welcome. Such tools speed up the process of selecting the converter by saving the designer the time and effort needed to develop a system just to evaluate the part. Besides having the converter chosen more quickly and easily, the design process should be further speeded up with a quick and easy means of testing the part in the application. To be useful, the test system should effectively be self-contained, run on a platform readily available to the designer, and fulfill two distinct functions: provide a quick means of demonstrating the performance of the converter, and provide a development platform for evaluation of the converter in the user's application.

Those were the design goals for an evaluation system for medium- and high-speed general purpose analog-to-digital converters, using a standard PC as the platform for evaluating the devices. The PC has two ports for external communications—a serial RS-232 port and a parallel printer port. Because neither port can operate at the speeds required to run an ADC at throughput rates in excess of 10,000s of samples per second, direct connection between the PC and the ADC is not possible if the ADC is to be operated at specified throughput rates.

Thus, to facilitate controlling the ADC and running it at specified speeds, additional processing power is required external to the PC. A memory buffer area is also required to store the data, gathered at the higher throughput rates, before it is uploaded to the PC at the lower rates compatible with its porting speed. One approach is to build evaluation boards with processing power and memory. But this has the disadvantage of requiring a processor on every evaluation board; and the evaluation board becomes less flexible for use as a development board.

The approach adopted by ADI's General-Purpose-Converter Applications Group in Limerick was to simplify the evaluation boards and move the memory, processing power and PC communications to a separate controller board. This controller board, labeled EVAL-CONTROL BOARD, provides the link between the RS-232 port of the PC and the evaluation board for the device of interest. It provides a means of controlling a converter's (daughter) board and operating a converter at its maximum throughput rate, while demonstrating the results on a PC. The Eval-Control Board is capable of being used with a suite of daughter evaluation boards, each geared to the specific needs of a particular converter or family. The user buys one Eval-Control Board and can connect daughter evaluation boards to this controller board via a standard 96-lead connector. The system configuration is shown in Figure 1.*

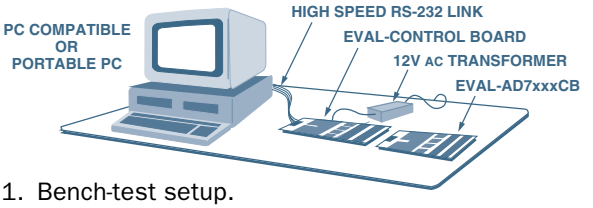


Figure 1. Bench-test setup.

All daughter evaluation boards that are compatible with the Eval-Control Board have designations that end with the letters CB. To date, there are 10 daughter ADC evaluation boards available for use with the controller board; their performance range is from the 12-bit, 600-ksps AD7892 to the 16-bit 200-ksps AD976A.*

In keeping with the requirement that the setup be self-contained, a standard 12-V ac transformer with 1-A current capacity is available to power the system. From it, the Eval-Control Board then generates all the power required for itself and the daughter board (Figure 2). The board's functions are based on an Analog Devices ADSP-2111 digital signal processor (DSP). The ADSP-2111 features two high-speed serial links, a 2K × 24 internal program-memory RAM and a 1K × 16 internal data-memory RAM. The processor controls the sampling rate and the data acquisition from the evaluation board. For serial interfaces, it is capable of taking data at a bit rate of 8 MHz; for parallel interfaces, it has a word rate of 3.2 MHz.

Communication between the Eval-Control Board and the PC is controlled by an 8051 microcontroller. The UART port on the 8051 connects to the COM-1 serial port of the PC, and information is transferred via a standard RS-232 cable. The 8051 is connected to the host interface port (HIP) of the ADSP-2111. The software for the appropriate daughter evaluation board is downloaded to the ADSP-2111 via the 8051. Similarly, when the ADSP-2111 has acquired and processed the data samples, they are transferred back to the PC for analysis via the 8051. The Eval-Control Board's 8K × 16 bit RAM allows as many as 4000 samples to be stored before they are transferred up to the PC for processing. It also includes a 14-bit single-chip DAC and ADC (AD7869). Thus it can acquire analog data, and generate analog output signals if the user so wishes.

The evaluation software, which runs under DOS 4.0 or higher, allows the user to control the operation of the daughter board,

*To request technical information on this system, **Circle 4**

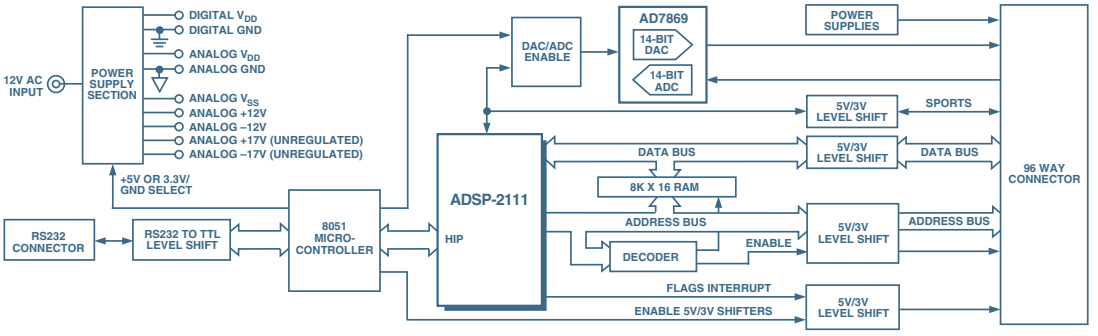
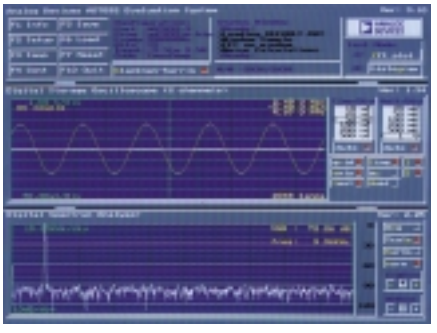


Figure 2. Block diagram of the Evaluation-Control Board.

which contains the device under test. The samples are gathered at rates up to the maximum throughput rate of the converter, and then uploaded to the PC for display and analysis. The front-end PC software has a number of screen displays; examples of these are shown in Figure 3.



a. Sine wave and its digitized spectrum.

b. Histogram analysis

Figure 3. Examples of data presentation.

The software runs with a series of function keys, hot keys and on-screen buttons. With it, the user can select sample rate, number of samples to be taken, analog input range, mode of operation and control of on-chip registers. The software can also perform a window function on the captured data, carry out a fast Fourier transform (FFT), compute signal-to-noise ratio, and display the results. It can also display the spread of codes for a dc input and compute the mean and standard deviation of the distribution. The software allows the captured data to be stored to a file, from which it can be exported for processing by other software packages. Data can be taken from a file (rather then captured from the evaluation board) and processed off line.

The Eval-Control Board thus fulfills its requirement of demonstrating nominal performance using the complete set of software routines for the above functions. Once the designer has moved to the evaluation phase, these routines can be adapted to evaluate the device under application-specific conditions. Here the Eval-Control Board can operate as a true development platform. To adapt and develop the software for this purpose, it is first necessary to understand how the software for the Eval-Control Board works.

SOFTWARE

The software comes in two main parts. The first, written in C code, runs on the PC; the second is the DSP code—it runs on the evaluation control board and is based on the ADSP-21xx code. We consider here as an example a 12-bit ADC with a parallel data bus. Before examining the 21xx code, one should understand what happens when the user selects commands from the PC software.

Each daughter evaluation board requires its own software routines; they are stored on the PC and downloaded to the Eval-Control Board whenever that specific evaluation board is to be used. The board-specific software files are called host-interface-port (HIP) files. When the user selects the program to be loaded, the HIP file for that program is loaded to the Eval-Control Board over the serial port of the PC. After a program has been loaded, the DSP program causes it to wait until it gets a command before doing any further operations. When the user selects an operation from the PC, a four-byte code is sent to the DSP via the serial port. The code is pre- and post-formatted with an "S" and "E" character respectively. These allow the software to interpret what function is required to be carried out (e.g., take samples, write to a register etc.) When a command is sent to the Eval-Control Board the 'S' and "E" bytes are stripped by the microcontroller and the 4 bytes are loaded into data memory (DM) addresses 0x3FE1, 0x3FE2, 0x3FE3 and 0x3FE4, as diagrammed here.

S	0x3FE1	0x3FE2	0x3FE3	0x3FE4	E

HIP Register Addresses

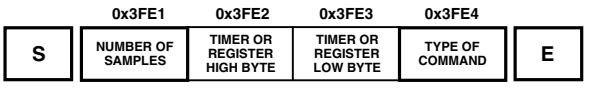
The microcontroller also writes a value of 0x03 to adö3ess 0x3FE0 to indicate that data has been received. These addresses are called the HIP registers. There is also a HIP status register at address 0x3FE6. This register is checked to see if any new data has been written to the HIP registers, by either the DSP or the PC. The four-byte code sent to the DSP can be seen if the command line option -e+ is added to the program name running on the PC. For instance, if the program being used is AD7892.EXE, the command line is AD7892.EXE -e+.

The first step in writing code for an application is to write all the initial setup routines for the DSP—the interrupt vector addresses, the serial port configurations and initialization of any flags that may be needed. (That part of the code, which depends on the specific application, will not be shown in this article.) Once the DSP has been set up, the program should wait for commands to

be sent to it from the user. This is done using the Wait_Confirm subroutine as shown below and ALU input registers AX0 and AY1. AR is the ALU output register.

```
wait_confirm:
  AX0=DM(0x3fe6);          {load HIP status register into AX0}
  AY1=0x0001;              {load AY1 to check HIP against register 1}
  AR=AX0 AND AY1;          {Has anything been written?}
  IF EQ JUMP wait_confirm; {If not then repeat the loop}
  RTS;                     {return when the commands are received}
```

This routine simply monitors the HSR6, HIP Status Register (0x3FE6) and doesn't return until the LSB of the register is a 1, indicating that something has been written to the HDR1 register. This diagram identifies the contents of the four data bytes:



HIP Register Functions

Once the data is received, the timer register can be loaded. The manipulation of the data to rebuild the 2 bytes into one 16 bit word (by shifting the high byte 8 bits left and combining), and store it in data memory, is shown here:

```
AX0=DM(0X3fe2);      SI=AX0; SE=8; SR=LSHIFT SI(LO);
AX0=DM(0X3fe3);      AY1=0X00ff; AR=AX0 AND AY1;
AX0=AR; AY1=SR0;     AR=AX0 OR AY1;
AY0=AR;AR=AY0-1;
DM(Tcount_Reg)=AR;  DM(Tperiod_Reg)=AR;
```

Finally, the address of the parallel port (in this case the edge connector), and the start address of the memory location where the data is to be put, need to be set up. This is done using the ADSP-2111's pair of data-address generators (DAGs). DAGs consist of three registers, identified as I (Base/index address of the memory block), M (incremental step to next location), and the L (the length of the memory block;The L block is required for return to start of a loop involving a circular buffer; in this example it will be set to zero). The code looks like this.

```
  I0=0; M0=1; L0=0;          {address of memory locations for data}
  I1=0x2000; M1=0; L1=0;     {address of parallel port }
```

A loop can now be set up which will read in a data sample every time an interrupt occurs. Since reading samples takes but a fraction of the time of the whole operation (i.e., reading and uploading the data) it is possible to fill the memory with data and only select a portion to upload.

```
  AY1=1;AR=8191;                {set sample increment and number of
                                 samples req'd}
  MSTAT=0x20; IMASK=0x01;       {start the timer and unmask the interrupt}
luup:  IDLE;                    {wait for the interrupt to occur}
luup1: AR=AR – AY1;             {decrease the count}
       IF NE JUMP luup;         {repeat until finished}
```

In this example the code is simplified to use only the timer interrupt. This can be done by waiting for the timer, starting from a preset time, to expire—thus causing an interrupt. Data can then be read from the data bus and, after a short delay (if required), start the next conversion. The code below shows how the timer interrupt vector address should look when it appears in the vector table. The interrupt service routine is also shown.

```
timer_int: jump ISR;RTI;RTI;RTI;  {interrupt vector}
ISR:   AX0=DM(I1,M1);             {read data}
       DM(I0,M0)=AX0;             {Write to memory}
       RESET FL0; SET FL0;        {Convst}
       RTI;
```

When using this technique the first data value to be returned must be ignored, because it will have been read in before the conversions were started; hence it is not valid. Once all the data has been read in, it is time to upload the data to the PC. After turning off the interrupts and resetting the DAGs controlling the data memory, one can check to determine how many samples are required to be uploaded, using this code:

```
  IMASK=0x00; MSTAT=0x10;     {mask all interrupts and stop the timer}
  I0=1; M0=1; L0=0;           {reset DAGs to start of Data Memory }
  AR=DM(0x3fe1); MY0=256; MR=AR*MY0(UU);
                              {Read number of samples required}
  AY0=MR0;                    {store count}
```

The data from the 12-bit ADC should be sign-extended to fit the 16-bit-wide data registers. This can be done by examining the data and, if the MSB is a 1, OR the data with 0xF000 to set the highest 4 bits to 1 as shown here.

```
MORE_TO_ECHO:  AX0=DM(I0,M0);     {read the data value}
AY1=0x800; AR=AX0 AND AY1;
IF EQ JUMP OVER;                  {check the MSB }
AY1=0xF000; AR=AX0 OR AY1;
AX0=AR;                           {if it's a 1 set the upper bits to 1}
```

The data is now properly formatted and can be transferred to the PC via the host interface port. This is done by calling the OUT_HIP routine as part of a loop:

```
OVER:          CALL OUT_HIP;            {upload the data value }
               AR=AY0–1;                {decrease the count }
               AY0=AR;                  {and copy it back to the
                                         register}
               IF GE JUMP MORE_TO_ECHO;
                                        {if we're not finished then
                                         repeat}
GG:            AX0=0x00FF;              {all the data has been
                                         so indicate this to the PC}
               DM(0X3fe3)=AX0;AX0=0;
               DM(0x3fe0)=AX0;
               JUMP cloop;              {return to start and wait for
                                         next command}
OUT_HIP        SI=AX0;   {input the data to the barrel shifter}
               SE=–8;    {set the number of bits to shift by}
               SR=LSHIFT SI(LO);        {and shift the data}
               DM(0X3FE4)=SR0;          { HI byte }
               DM(0X3FE5)=SI;           { LO byte }
               AX0=1; DM(0X3FE3)=AX0; { indicate that data
                                          is available }
               CALL WAIT_UPLOAD;        {and upload it to the PC}
               RTS;                     {return when finished }
WAIT_UPLOAD:   AX0=DM(0x3FE6);          {check contents of HIP
                                         register 6}
               AY1=0x0001;
               AR=AX0 AND AY1;
               IF EQ JUMP WAIT_UPLOAD; {repeat until ready}
               AX0=DM(0x3FE0);
               AY1=0x0003;
               AR=AX0 - AY1;
               IF NE JUMP WAIT_UPLOAD;
               RTS;
```

Once the required number of samples has been sent to the PC, the program should return to the start of the main loop and wait for further instructions.

The last few routines are the standard set; they will rarely need to be changed when modifying the Eval-Control Board's DSP code to meet application-specific conditions. All the routines shown above have been used in the HIP files that control the various evaluation (daughter) boards that interface to the PC via the Eval-Control Board. They are shown here to give an indication of how existing programs are modified for additional functionality.

Build a Smart Analog Process-Instrument Transmitter with Low-Power Converters and a Microcontroller

By Albert O'Grady & Jim Ryan.

An analog transmitter is a field-mounted device that senses a physical parameter such as pressure or temperature and generates a current proportional to the measured variable in the standard range, 4 to 20 mA. Providing the output as a current in a twisted-pair loop has many advantages: the measurement signal is insensitive to noise and is not affected by changes in loop resistance; transmitters meeting the standard are interchangeable; and the power required to energize the transmitter circuits can be derived from a remotely supplied loop voltage. Figure 1 shows a conventional transmitter circuit, consisting of a power supply, a current-manipulating transmitter, and a receiving controller.

Figure 1. Analog Transmitter.

Transmitter design has responded to the requirements of users for improved performance and versatility, plus reduced cost and maintenance. A second-generation "smart analog transmitter" has a microprocessor (and data conversion), to provide remote memory and computing power (Figure 2). It can condition the signal remotely before converting it to current and transmitting it back to the controller. For example, it can normalize gain and offsets, linearize sensors having known nonlinearities (such as RTDs and thermocouples) by converting to digital, processing with arithmetic algorithms in the µP, converting back to analog and transmitting on the loop as a standard current. This reduces the control room's signal processing burden, a big advantage if a large number of signals must be dealt with.

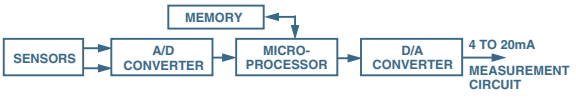


Figure 2. Smart Transmitter.

The third generation, "smart-and-intelligent" transmitters, add digital communications, which share the same twisted-pair line with the traditional 4-20-mA "dc" signal (Figure 3). The communication channel allows both analog and digital versions of the measured variable to be transmitted over the twisted pair, as well as control signals and diagnostic data relevant to the transmitter, such as calibration coefficients, device ID, and data relevant to fault diagnosis. Transmitter faults can be diagnosed remotely—very useful for transmitters in hazardous locations.

The Hart protocol is the *de facto* communication standard used by smart transmitters. It employs frequency-shift keying (FSK) modulation, based on the Bell 202 Standard. Data is transmitted at 1200 bits/s, switching between 2.2 kHz ("0") and 1.2 kHz ("1"). (See sidebar, page 15.)

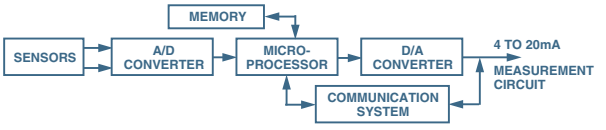


Figure 3. Intelligent Transmitter.

Component selection for smart analog transmitter designs: Figure 4 shows a circuit that implements the smart transmitter of Figure 2. The following sections discuss smart transmitter design factors and tabulate alternatives. Besides low cost, the all-important constraint is that the entire circuit consume less than 3.5 mA (the "low alarm" setting, 0.5 mA below the 4-mA signal floor), to permit the transmitter to be loop-powered.

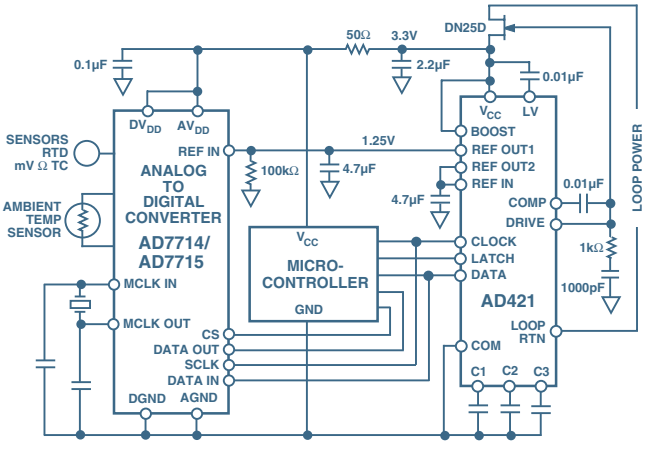


Figure 4. Details of a Smart Transmitter.

A/D converter: Other major criteria for ADC selection are:

- a high level of integration to reduce front-end component count
- high resolution to meet required system resolution & accuracy
- Single-supply operation on either 3-V or 5-V supply
- Calibration features to allow the removal of component or system errors due to drift with time and temperature.

The AD7713, AD7714, and AD7715 meet these criteria and are suitable for use in the front end of any smart transmitter.

The **AD7714** is a complete multi-channel (3 differential, 5 single-ended) analog front end targeted for low-frequency applications. It can accept low level signals directly from the transducer (Figure 5), has an on-chip programmable-gain amplifier (PGA), configurable for gains from 1 to 128. Front-end instrumentation amplifiers are unnecessary in most applications using the AD7714.

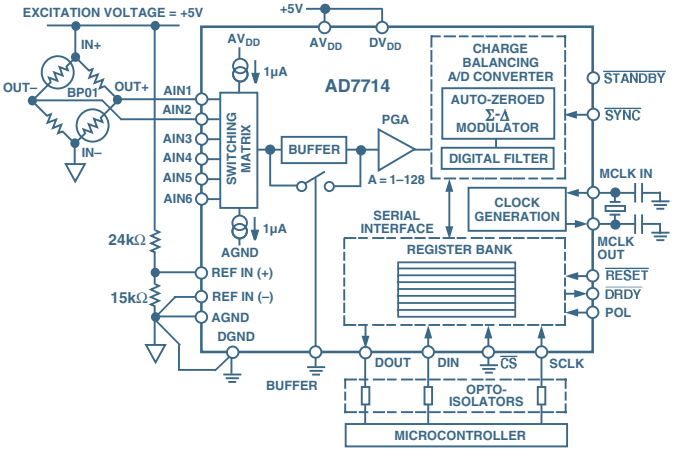


Figure 5. Interfacing a transducer interface to AD7714 ADC.

The reference can be derived from the sensor excitation voltage for ratiometric measurement applications.

Its sigma-delta architecture is capable of up to 24 bits of no-missing-codes performance. Operation is from a single 3- or 5-V supply, consuming 650 μA (< 5 μA in power-down mode). The AD7714 has a differential reference input. Its input signal range is from 0 to +20 mV up to 0 to +2.5 V, unipolar, depending on the PGA gain setting, and ±20 mV to ±2.5 V bipolar. Its serial interface can be configured for easy-to-isolate 3-wire operation by a microcontroller in a smart transmitter circuit.

The μC can do calibrations periodically, removing gain and offset errors—and drifts with time and temperature—in the device itself or the whole system. The calibration features include self-, background-, & system calibration. On-chip calibration registers allow OEMs to do calibrations at the factory, store coefficients in memory, and rewrite them to the device in the field.

The **AD7715** is essentially a 16-bit, 1-channel version of the AD7714, with all of its features, including the PGA and input signal ranges, differential reference, calibration features, 3-V or 5-V single-supply operation, and 3-wire serial interface.

The AD7713 is a 24-bit complete analog front end for low-frequency measurements. Its two low-level differential analog input channels can take signals directly from a transducer. It also accepts a high-level (up to four times the reference) single-ended input. It has a differential reference input, and two on-chip current sources are available; they can be used for excitation in 3-wire and 4-wire resistance temperature detector (RTD) circuits. Gain settings, signal polarity, and RTD current control can be configured in software using the bi-directional serial port. The AD7713 is also capable of self calibration, system calibration and background calibration to remove zero- and full-scale errors.

ADC Selection Table†

ADC	Resolution	Input channels	Supply voltage	Current consumption*	Package options
AD7714	16/24	3 fully differential or 5 single-ended	3 V/5 V	500 μA @ 3 V 670 μA @ 5 V	24-pin DIP, 24-lead SOIC, 28-lead SSOP
AD7715	16	1 fully differential	3 V/5 V	450 μA @ 3 V 650 μA @ 5 V	16-pin DIP, 16-lead SOIC
AD7713	16/24	2 fully differential and 1 single-ended	5 V	1.1 mA	24-pin DIP, 24-lead SOIC

*Current consumption values are based on using a 1-MHz master clock.

†For technical data on these devices, consult our Web site, **www.analog.com**, use Faxback (see p. 24), or circle **5**

Microcontroller: The microcontroller (μC) is the engine of the smart transmitter; it controls the entire transfer of information from sensors to loop current. The μC's memory and processing capability makes possible periodic calibrations, signal conditioning, error correction, temperature compensation, and linearization, all at a remote location powered by loop voltage. Besides low cost and low power consumption, a μC for a smart transmitter should have these features:

- memory. It should contain enough ROM and RAM for implementing all software functions (boot program plus data processing) without external memory; this reduces component count, board space and power consumption in the system.
- serial communications port to provide an internal interface with the input ADC and the output DAC for control and data transfer. Galvanic isolation is easily implemented with a few optoisolators.
- low clock speed to minimize power consumption, which is generally directly proportional to clock speed in CMOS devices.

The table suggests μCs with sufficient on-chip memory and low-enough power consumption to be powered from the loop and to implement the "smart" functions required by a typical transmitter.

Microcontroller Options

Micro-controller*	On-chip ROM	On-chip RAM	Power consumption
80L51	4K × 8	128 bytes × 8	1.7 mA (Vcc=3 V, Fclk=3.58 MHz) 50 μA (Vcc=3 V, Fclk=32 kHz) 10 μA typ in power-down mode
MC68HC05	6160 bytes	224 bytes	0.8 mA (Vcc=5 V, Fclk=100 kHz) 0.7 mA (Vcc=3 V, Fclk=100 kHz) 32 μA @ 5 V, 20 μA @ 3 V in power-down
PIC LC 54	512 bytes EEPROM	25 bytes	1.8 mA(Vcc=5 V, Fclk=4 MHz) 14 μA (Vcc=3 V, Fclk=32 kHz 5 μA in power-down mode
MC68L11	16K	512 bytes	2 mA (Vcc=3 V, Fclk=500 kHz)
μPD780xx	8K to 32K	256 bytes to 1024 bytes	120 μA(Vcc=5 V, Fclk=32 kHz) 64 μA (Vcc=3 V, Fclk=32 kHz) 1.8 mA (Vcc=3 V, Fclk=5 MHz)

*These microcontrollers are not Analog Devices products.

D/A converter: In the smart transmitter, the DAC is the means of driving and controlling the loop current. The examples we will consider here involve 2-wire, remotely powered transmitters.*

The D/A converter and current loop control circuitry should have comparable resolution to the front-end conditioning circuitry and the ADC; and the DAC should be monotonic, since the process variable (PV) may be part of a control loop. These, together with supply current low enough to keep the total remote drain from the loop supply below 3.5 mA, are the minimum requirements. The specified current drain of the DAC circuit must of course include that of a precision reference and the quiescent current of an output amplifier. Operating temperature range must be sufficient to maintain required overall specifications without excessive drift in an industrial environment. Other requirements:

- A highly integrated chip for overall component reduction
- High resolution to meet system resolution and accuracy needs
- Single-supply operation on either 3-V or 5-V supplies.

The AD421 and AD422 monolithic ICs are designed specifically for industrial current-loop control applications. Both devices offer the functions essential to remote transmitter operation.

The **AD421*** is a loop powered current-control sigma-delta DAC, implemented in BiCMOS, for high resolution and accuracy. It is complete with two precision references and a voltage regulator. The DAC has 16 bit resolution for operation in the 4-to-20-mA (16-mA span) program range, and an extra bit for optionally programming alarm currents in the range 0-32 mA. The DAC output provides the setpoint to a loop-current control circuit within the AD421. This circuit servoes the loop current to track its setpoint by measuring the return current and manipulating the current drawn at its Boost terminal. The 1.25-V and 2.5-V precision references, laser trimmed and temperature compensated for low drift, eliminate any need for stand-alone references. They can be used as reference inputs to the DAC (2.5 V) and an ADC.

The AD421 incorporates an adjustable voltage regulator, which powers the whole remote transmitter circuit, including the AD421 itself. The regulator has selectable settings for 3-V, 3.3-V and 5-V

*In most industrial applications power and signals (or process variables) share the same wiring to remote locations. The 4-20-mA interface can be used either to transmit measured variables or to send a command signal to a valve or actuator. Actuators may use more power than can be effectively derived from a 4-20 mA loop signal, so they are normally connected as four-wire devices, two for command signal and a separate pair for powering the device.

operation, and can be programmed to any voltage from 3 to 5 V with a suitable external resistor. An external depletion-mode pass transistor is required to implement this regulator function; it must be capable of supplying the total current required by the transmitter. The AD421 is available in a small-outline surface-mount package, which fits nicely in crowded explosion-proof housings.

Besides the advantages of integration, another benefit is that the device's current-loop control performance is specified, avoiding the need to calculate error budgets involving multiple devices. The AD421 features an SPI type three-wire interface that allows easy and efficient interface to most microcontrollers and requires a minimal number of opto-isolators if galvanic isolation of the loop from the transducer is needed for intrinsic safety.

The AD421 was designed for use in both smart and intelligent transmitter applications. Smart transmitters (Figure 4), though digital in operation, simply produce analog loop current proportional to process variable over a 16-mA (4-20-mA) span. Intelligent transmitters add another dimension of functionality (see sidebar). The transmitter can both send a PV signal on the current loop in analog form, and it can transmit and receive digital information by modulating the current in the loop. The digital signals are sent and received using a modem circuit, which translates and transmits digital levels as modulated currents and translates received modulated current into digital ones and zeros. The AD421 can be interfaced with a stand-alone modem; its current control loop section provides a suitable input node for the modulation signal to be coupled from an external HART modem, such as the AD424 or the 20C15 from Symbios Logic. The separate modem is digitally interfaced to the microcontroller or a UART, as shown in Figure 6.

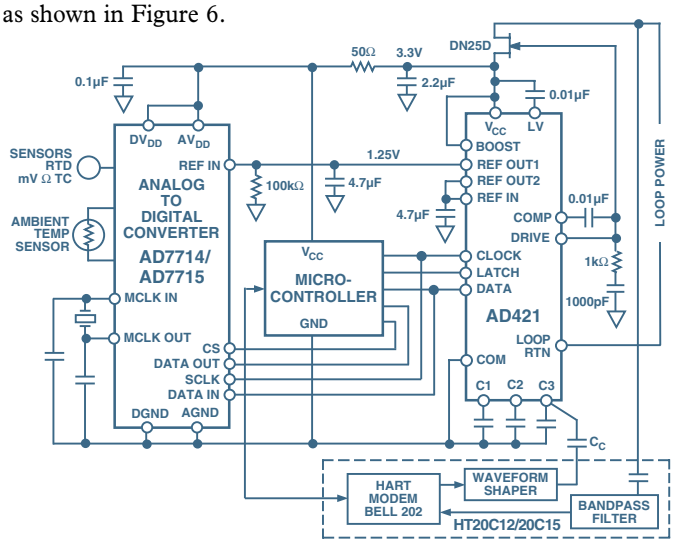


Figure 6. Complementing the smart transducer of Figure 4 with a discrete HART modem.

A new device, the **AD422**,* reduces the physical complexity of intelligent transmitters using the HART protocol. It combines the AD421's functional blocks (voltage regulator, DAC, current control loop and references) with a HART modem and several supervisory circuits (watchdog timer, alarm input and reset generator)—all on a single chip! It is a highly integrated solution specifically targeted to design of intelligent transmitters (Figure 7), with a greatly reduced component count.

*For technical data on the AD421 and AD422, consult our Web site, **www.analog.com**, use Faxback (see p. 24), or circle **6**

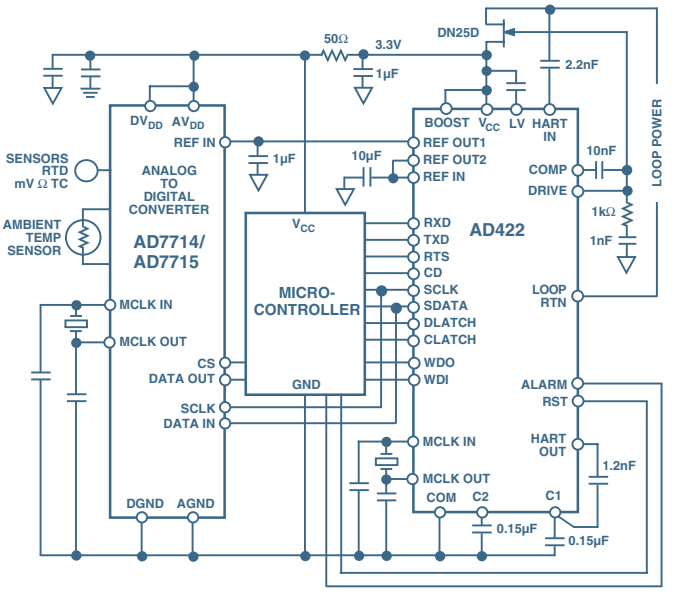


Figure 7. Complete intelligent transmitter with AD422

HART PROTOCOL

The *de facto* standard for communication over 4-to-20-mA current loops in industrial applications is the Highway Addressable Remote Transducer (HART) protocol, originally developed by Rosemount, Inc., but now supported for the general community by the HART Foundation. The protocol is adapted from the Bell 202 frequency-shift keying (FSK) telephony standard: the loop current is transmitted at 1200 bits/second as one of two phase-continuous frequencies, 1.2 kHz—"mark" (1) or 2.2 kHz—"space" (0). Suitably filtered, the ac signals do not affect the measurement's dc value. HART implements a *master/slave* protocol; a remote "slave" device responds only when addressed by the master.

As smart transmitters are remote instruments with no means of communication other than the analog PV signal, they could not be interrogated for status information (but an extra alarm bit is available to output currents less than 4 mA or greater than 20 mA). Intelligent transmitters, however, can communicate with the control room interactively so that detailed status information can be polled at any time. HART circuitry can replace an existing smart or analog transmitter installation without having to run new cabling—a major advantage because a large proportion of existing transmitter installations can be upgraded simply by replacing the existing transmitters with HART-compatible transmitters. The intelligent transmitters also allow the performance of process control loops to be improved. For example, the control room can remotely "trim" the transducer output. Transmitters are often capable of measuring two process variables (primary and secondary process variables) instead of the single PV that can be transmitted via a simple 4-to-20-mA interface. Intelligent transmitters can send information on two PVs, plus other relevant information. HART configurations can also feature digital communication alone; the analog current is used solely as a vehicle for the digital information.

The protocol has many layers closely related to the seven-layer OSI model. The AD422 from Analog Devices is a solution at the physical layer; the others are implemented in software.

New Product Briefs (For information use reply card or see back cover)

Amplifiers, Buffered Switches & Muxes

4-μA Op Amps

Dual OP281 & Quad OP481
Rail-rail outputs, 1-mV V_{OS}

The OP281 and OP481 respectively comprise one and two pairs of very low power op amps having fast recovery times (useful in comparator applications) sink/source outputs without increased supply current when at the rails. Maximum supply current is 4 μA per amplifier (5 μA from –40 to +85°C). Operation is guaranteed with single supply from 2.7 to 12 V, and the devices are specified at +3, +5, and ±5 V.

The low power consumption enables operation for years on batteries, for remote sensors, and for applications such as security systems and medical instrumentation. The OP281 is available in 8-pin DIP, SOIC, and TSSOP packages; the OP481 is available in 14-lead DIP, TSSOP and narrow-body SO. Prices (1000s) start at $2.44 for the duals, $3.19 for the quads.

Faxcode 2075* or Circle 7

Ultrafast Op Amp

AD8009 has 1-GHz BW
5500 V/μs SR, 175 mA Output

The AD8009 is an unusually fast, low-distortion monolithic current-feedback operational amplifier, characterized by 1-GHz typical small-signal bandwidth (G=+1), 440-MHz large-signal bandwidth (G=+2), 5500-V/μs slew rate, and 10-ns settling time to 0.1%. It has a SFDR of 44 dBc at 150 MHz and a 3rd-order intercept of 18 dBm at 150 MHz.

It can furnish 175 mA of load current, will drive 4 back-terminated video loads, and has excellent video specifications, viz., differential gain and phase errors of 0.01% and 0.01°, with 150-Ω load. The AD8009 operates at ±5 V, drawing about 14 mA. Typical applications are in pulse handling, video, RF/IF, and high speed test and instrumentation. Housed in an 8-pin SOIC, it operates over the –40 to +85°C range. Price in 1000s is $2.99

Faxcode 2079* or Circle 8

6×16 Video Switch

256-point, 200-MHz AD8116:
Crosspoint has output buffers

The AD8116, the world's first 16 × 16 video crosspoint switch IC, and the first of a family, routes video signals from any of its 16 inputs to any of its 16 buffered outputs (which are 3-statable and can drive 150 Ω), as programmed by an 80-bit serial word. It has –3-dB bandwidth of 200 MHz and switching time of 60 ns for 0.1% settling. It can route many types of signals, including compressed or uncompressed composite or component video signals. Its uniquely high speed and compact size are helpful for building large wideband switch arrays. Applications include broadcast video, surveillance and video conferencing, video on-demand, and inflight entertainment.

It is packaged in a 128-lead TQFP (14 mm × 14 mm) and is specified for 0 to +70°C. It requires a ±5-V supply, and dissipates only 900 mW. Prices start at $105 in 100s.

Faxcode 2070* or Circle 9

xDSL Driver/Receiver

Differential 500-mA drivers,
Low-noise preamplifier pair

The AD816 comprises two 500-mA current drivers and two low-noise (4 nV/$\sqrt{\text{Hz}}$) voltage-feedback amplifiers (with 70-mA drive capability), combining drive and preamplification on a single monolithic chip. It functions as the line interface to and from the telephone line in telecommunications applications such as ADSL, providing up to 26 dBm of differential line drive. It can also be used in CRT monitors, and its voltage-FB amplifiers are useful in active filters.

The thermally overload-protected driver can apply 40 V p-p differential output to a 50-Ω load at 1 MHz or furnish 1 A of peak current to a 15-Ω load with a 1% duty cycle. The AD816 is available in low thermal resistance power packages, operates from –40 to +85°C, and is specified with ±15-V supplies, drawing 59 mA max of quiescent current. It is priced at $7.25 in 1000s.

Faxcode* 1978 or Circle 10

VGA: Linear Gain (dB)

AD604/605 duals have low
noise, 40-MHz bandwidth

The AD604 and AD605 are high-performance wideband (40-MHz) 2-channel variable-gain amplifiers (VGA). Gain is linear in dB as a function of control voltage. They can be used to control signal gain & attenuation in AGC applications or as a time-gain amplifier in medical ultrasound. The **AD604,** optimized for low noise (0.8 nV/$\sqrt{\text{Hz}}$ RTI), offers gain ranges from 0 through +48 dB and +6 through +54 dB. In addition, control-voltage sensitivity can be scaled from 20 dB/V through 40 dB/V. The single-supply **AD605** has gain ranges of –14 to +34 dB and 0 dB to +48 dB.

They are available in plastic DIP and SOIC packages for operation from –40 to +85°C. The AD605, available in A and B grades, has 16-pins; the AD604, operating from ±5-V supplies, has 24 pins. AD604/605 price in 1000s starts at $11.90/$8.90.

Circle 11

Fast Buffered Muxes

700-MHz AD8170/74 (2:1/4:1)
750-MHz '80/'82 (2:1, 2×2:1)

The AD8170, -74, AD8180, and -82 muxes select between wide-bandwidth input signals, and switch them in <10 ns. Typical applications are in large video switcher and router arrays, scanners, picture-in-picture video, and MPEG video for PCs. All four devices have buffered inputs & outputs. The **AD8174** switches 4 signals; the **AD8170** switches 2 signals, with a 250-MHz BW (G=+2). In both, a current-feedback amplifier buffers the output; its gain can be set with external resistors. The **AD8180** switches two signals with a bandwidth of 750 MHz; the **AD8182** is a dual 2:1.

Power consumed is low (±5 V,<10 mA), but the '7x deliver >50 mA and the '8x deliver >30 mA. They operate from –40 to +85°C, are housed in 8- and 14-lead PDIPs and SOICs. Prices (1000s) are $1.95/$2.95 ('80/'82) and $2.25/$3.95 ('70/'74).

Circle 12

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

A/D and D/A Converters, Volume Controls

12-Bit μpower D/A

2.7 to 5.5-V, 100-μA rail-rail AD7392/93: pin-compatible

With a maximum I_{DD} of 100 μA, the 12-bit AD7392 and 10-bit AD7393 are the newest members of a family of DACs having ultra-low power consumption. Operating on a 2.7 to 5.5-volt single supply, they offer a pin-compatible choice of parallel-loading 12 or 10-bits, allowing a cost/resolution tradeoff without board layout changes. Typical dissipation in 3-V operation is 165 μW; in shutdown, supply current drops to 0.1 μA.

The output range is rail to rail (0 to V_{DD}), and the (multiplying) reference input can be tied to VDD. Both devices are available for –40 to +85°C. Packaging is in 20-pin PDIPs and SOICs; AD7393 versions are also available in a 1.1-mm high tiny TSSOP-20, for PCM card applications, and in a SOIC for –40 to +125°C for automotive applications. Prices (1000s) start at $2.95 for the AD7393 and $5.06 for the AD7392.

Faxcode* 2068 or Circle 13

Two 16-Bit, +5-V ADs

AD7722: Σ-Δ, serial/parallel AD976/A: 2× faster 2nd source

The **AD976**, pin-compatible with the **ADS8705**, is a 16-bit low-power +5-V single-supply successive-approximation ADC. It samples at up to 100 ksps, and the **AD976A** version samples at 200 ksps. The device has an on-chip clock and 2.5-V reference, accepts inputs up to ±10 V, and dissipates only 100 mW. Operation is from –40 to +85°C. Packaging is in 28-pin DIP, SOIC, and SSOP, and prices for AD976/A in a plastic DIP (1000s) are $20/$26.

The **AD7722** is a complete sigma-delta ADC with signal bandwidth up to 100 kHz and output word rate up to 220 ksps (14-MHz clock). It has an on-chip reference and can interface in either parallel or serial mode (a pair of converters can share the serial bus). Input range is 0 to +2.5 V or ±1.25 V. It draws 375 mW, is available in a 44-pin PQFP for –40 to +85°C. Price (1000s) is $20. For data on both ICs, **Circle 14**

8-Bit, 200 MSPS ADC

AD9054 uses only 500 mW, has 380-MHz full-power BW

The AD9054 is an 8-bit monolithic A/D converter optimized for high speed, low power, small size, and ease of use, using an innovative bit-per-stage folding architecture with many advantages over traditional "flash" converters. Its output is interleaved between two TTL-compatible output ports at one-half the clock rate, reducing interface speed and buffer memory cost. 80-MHz SINAD (200 MSPS) is 43 dB. Applications include RGB video processing, digital data storage read channels, medical imaging, direct-IF & undersampling in digital communications.

It operates on a single +5-V supply and has an internal 2.5-V reference. The analog input range is 1 V p-p. Two speed grades are available in a 44-pin TQFP—200 MSPS and 135-MSPS sample rates. Respective prices in 100s are $48 and $28.

Faxcode* 2093 or Circle 15

12-Bit A/D Choices

Simultaneous dual AD7862 Single serial 3.8-μs AD7895

The monolithic **AD7862** comprises two 250-ksps 12-bit simultaneous sampling ADCs, each with multiplexed dual inputs. It includes an on-chip reference and parallel digital interface and requires a +5-V supply (60 mW dissipation, 50-μW in power-save mode). Available grades are A & B (–40 to +85°C) and S (–55 to +125°C). There is a choice of ±10, ±2.5, and 0 to +2.5-V input ranges. Housing is in PDIP, SO, SSOP, & Cerdip. Prices (1000s) start at $11.

The **AD7895** is a fast 12-bit single-supply ADC (+5-V, 20-mW) with automatic power-down. It converts in 3.8 μs and has a high-speed, easy-to-use serial interface. It is available in 8-pin mini-DIP and SOIC for –40 to +85°C in A/B grades, and a choice of ±10, ±2.5, & 0 to +2.5-V high-impedance-input ranges. Price (1000s) is $4.95/$6.80.

For data on both devices and 14-bit upgrades (AD7863 & AD7894), **circle 16**

Triple 8-Bit Video D/A

360-MHz, 196-bit ADV7129 Complete with PLL and V ref

The ADV7129 is a complete analog-output video DAC on a single CMOS chip, designed to drive ultra-high-resolution (2 K × 2 K) color monitors. It includes three 8-bit video DACs (RGB), a programmable pixel port, and an internal voltage reference. An on-board phase-locked loop clock generator provides high-speed operation without requiring high-speed external crystal or clock circuitry. The 192-bit input port enables full 24-bit true color pixel data to be displayed at pixel speeds of up to 360 MHz.

Its analog outputs are RS-343A/RS-170 compatible, and its digital inputs are TTL-compatible. It is fully controlled through its 8-bit MPU port by on-board command registers. It uses a single +5-V supply, has an internal voltage reference, and is available in a 304-pin PQFP package for 0 to +70°C. Its price in 100s is $765.

Faxcode* 1854 or Circle 17

Vol/Bal-Control ICs

6, 4-channel SSM2160, 2161 Clickless operation, serial in

The SSM2160 and SSM2161 are complete 6- and 4-channel clickless digital volume and balance control ICs. They accept 6 (or 4) audio signals and either amplify (up to 31 dB) or attenuate (over 100 dB) each one. A Master Control sets the attenuation, while a Channel Control enables balance to be adjusted. They are principally applied as the main volume/balance controller for a DVD player, multi-channel audio amplifier, hi-fi receiver, professional sound mixer, or communications voice processor.

Audio characteristics include THD+N of 0.01% and 0.001% IMD. Both devices can operate from single or dual supplies; e.g., the SSM2160 operates from +10-V to +20-V single supplies or ±5 to ±10-V dual supplies. They are available in PDIP and SO packages for 0 to +70°C operation. Prices (large quantity) are as low as 60¢/channel.

Faxcode* 1848 or Circle 18

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

New Product Briefs (For information use reply card or see back cover)

Power Management Supervisory Circuits

Step Up/Step Down

ADP3000 switching regulator
Micropower, high-frequency

The ADP3000 is a versatile step-up/step-down switching regulator that operates from an input supply of 2 to 12 V in *boost* mode and up to 30 V in *buck* mode. An adjustable and 3 standard fixed-output versions are available for 3.3, 5, and 12 V. The 3.3-V version can deliver an output current of 100 mA at 3 V from a 5-V input in step-down, and 180 mA at 3.3 V from a 2-V input in step-up configuration.

Few external components are required; and operation at a high switching frequency (400 kHz) allows the use of small inductors and capacitors. Operating in the pulse-frequency mode (PFM), it consumes only 500 µA. It has an on-chip low-battery detector, and the output current limit is user-settable. The ADP3000 is available in 8-pin DIP and SO-8 packages for 0 to +70°C. Prices (1000s): $2.14/$2.28 (PDIP/SOIC).

Faxcode* 2028 or Circle 19

Batt-Chge Controllers

Secondary side off-line
ADP3810/11: LiIon/NiCd, NiMH

The ADP3810 and ADP3811 precision battery-charger controllers combine user-programmable current limiting and precise voltage control to charge lithium-ion, nickel-cadmium, and nickel metal-hydride batteries (popular batteries for portable computing and communications gear). They combine a precision 2-V reference, control input buffer, under-voltage-lockout comparator, output buffer, and over-voltage comparator in an 8-pin SOIC for –40 to +85°C.

Charging currents are programmable from typically 100 mA to 1.1 A. The **ADP3810** features on-board precision resistors for ±1% overall accuracy when charging Li-ion batteries; it is optionally available for 4.2, 8.4, 12.6, and 16.8 V. The **ADP3811** is programmable via external resistors, for a wide range of user-selected voltages. Prices (1000s) are $2.57/$2.43, respectively.

Faxcode* 2069 or Circle 20

1-30 Volt Supplies

Step-up, step-down, fixed or adjustable µpower sw. regs.

The ADP1110 and ADP1111 are members of a family of step-up/step-down switching regulators with 3.3, 5, and 10-V fixed outputs, as well as adjustable-output versions. The 5-V, 10-V, and adjustable versions are pin-for pin replacements for existing 1110 and 1111 devices; the 3.3-V versions are currently available only from Analog Devices. The **ADP1110** has an input supply range from 1.0 to 30-V, permitting use on single cell batteries; the **ADP1111**'s input range is from 2-12 V in step-up, and 2-30 V in step-down.

Typical applications for the ADP1110 are in cellular telephones, pagers, cameras, laser-diode drivers, and handheld inventory computers. Both devices are available in 8-pin plastic DIPs and SOICs for operation from 0 to +70°C. Prices in 1000s for PDIP/SOIC are $2.42 /$2.57 for ADP1110, $1.93/$2.07 for ADP1111. **Circle 21**

Switching Regulators

High-efficiency synchronous
ADP1148 step-down family

The ADP1148 is a high-efficiency (>95% at 200 mA) synchronous step-down switching regulator with operating supply range from +3.5 V to +18 V. It is available for 3.3-V, 5-V and adjustable outputs; the 5-V and adjustable versions are pin-for-pin replacements for existing 1148 devices; the 3.3-V version, for use in low-voltage systems, is currently available only from Analog Devices. The ADP1148 switches a pair of external complementary MOSFETs at frequencies up to 250 kHz.

The ADP1148 has an automatic power-saving sleep-mode (2 mW at 10 V in) when load current drops below the level required for continuous operation. In logic-controlled shutdown mode, only 20 µA are required. The ADP1148 is available in 14-pin PDIPs and SOICs for –40 to +85°C. Respective prices (1000s) are $3.18/$3.31.

Faxcode* 2023 or Circle 22

µP Supervisory ICs

Low-cost ADM708ARM
Available in µSOIC packages

The ADM708ARM is a low-cost µP supervisory circuit for monitoring +5-V supplies/batteries and microprocessor activity. It is the first of the ADM70x family to be available in a tiny 8-pin µSOIC package (one-half the area of an SO-8). It provides a pre-trimmed 4.4-V power-fail reset, manual reset de-bounce, and reset pulse-generator for a microcontroller. It is complete, requires no external components, and draws only 200 µA of quiescent current.

It can be used in all kinds of microcontroller applications, including printers, modems, PC settop boxes, drives, telecom cards, routers, etc., and is well-suited for mobile applications. Its electrical specs are the same as those of the ADM708AR, and it is form, fit, and function-compatible with 708CUA. The ADM708ARM is specified for –40 to +85°C. Price in 1000s is $0.84 (i.e., 84¢!)

Faxcode* 1866 or Circle 23

µP Supervisory ICs

ADM690AA, ADM691AA
Now in SO, µSOIC & TSSOP

The ADM690A and ADM691A are the first small-package versions in the ADM69x family of microprocessor supervisory circuits. (More are coming!) The **ADM690** is now available in 8-pin DIP (-AAN), SOIC (-AARN), and µSOIC (-AARM); the **ADM691** is available in 16-pin DIP (-AAN), wide SOIC (-AARW), narrow SOIC (-AARN), and TSSOP (-AARU).

The functions of both devices include Watchdog timer, V_{CC} Reset, Automatic backup battery power switching, and Power fail monitoring. In addition, the AD691A's design includes fast onboard gating of Chip Enable signals and low line status indication. All A version devices allow the Vbatt terminal to float when not connected. All versions operate from –40 to +85°C. Prices are low, starting at (1000s) $1.44 (ADM690AARM) and $1.60 (ADM691AARM).

Circle 24

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

Mixed Bag: Communications, Video, DSP

Low-Cost SHARC

ADSP-21061: 120 MFLOPS 1 Mbit dual-ported SRAM

The ADSP-21061 is the first in a family of low-cost SHARC™ (Super Harvard ARchitecture Computer) DSPs. It features a high-performance 120-MFLOPS/120 fixed-point MOPS core. Its 1 Mbit of dual-ported on-chip SRAM stores up to 32 K 32-bit words. To eliminate bus bottlenecks, six DMA channels support background I/O transfers. An integrated host interface supports 16-bit or 32-bit µP. Two high-speed serial ports (40 Mbits/s) interface to industry-standard peripherals. The ADSP-21061 is pin-compatible with and runs the same source code as other SHARC DSPs.

It is a high-performance solution for price-sensitive applications in audio, graphics, communications, video, conferencing, and imaging. Development support packages and samples are available now. ADSP-21061 prices are $64 in 1000s, $49 in 10,000s.

Circle 25

CCD Signal Processor

AD980x: 12/10-bit, 6 MSPS Complete on a chip, PQFP-64

The AD9807/AD9805 is a complete single-chip charge-coupled-device (CCD) imaging decoder and signal processor. It integrates all of the signal conditioning and correction needed for most mid-range scanner applications. Its three color-component inputs can be directly ac-coupled from the CCD, and its output is a processed 12/10-bit parallel word. Included is circuitry to perform 3-channel correlated double sampling (CDS) and adjustment of the programmable gain. After conversion to digital, on-board DSP circuitry corrects for pixel rate offset and gain, and odd/even CCD register imbalance errors. A parallel control bus acts as a simple interface to µCs.

Operation is specified from 0 to +70°C on +5-volt analog and digital supplies, with dissipation of 530 mW max and packaging in a 64-pin PQFP. Its price in 1000s is $25.

Faxcode* 2021 or Circle 26

GSM Receiver IF

AD6459 is a 3-V subsystem: Mixer, Linear amp, I/Q Demod

The AD6459 is a 3-V, low-power receiver IF subsystem. Optimized for operation in GSM, DCS1800, and PCS1900 receivers, it is used in digital communication systems (cellular, satellite, and private mobile radio) to convert a signal from a high IF (up to 500 MHz) to a lower IF (5 MHz to 50 MHz), amplify the signal, and provide demodulated I and Q outputs. It consists of a mixer, an IF amplifier, I and Q demodulators, a phase-locked quadrature oscillator, a precise AGC subsystem, and a biasing system with external power-down.

It interfaces to AD7013, AD7015, and AD6421 baseband converters, will operate on supplies from 2.7 to 5.5 V, and draws 8 mA at mid-gain (and only 2 µA in Sleep mode). It is packaged in a 20-lead SSOP for operation from –25 to +85°C (–40°C for supply ≥3.3 V). Its price (1000s) is $5.95.

Faxcode* 2079 or Circle 27

Video Encoder

AD724: RGB to NTSC/PAL PLL helps reduce system cost

The AD724 is a low-cost RGB to NTSC/PAL encoder; it converts red, green, and blue color component signals into their corresponding luminance (baseband phase and amplitude) signals in accordance with either NTSC or PAL standards. It also makes available composite video output. All 3 outputs can simultaneously drive 75-Ω, reverse-terminated cables. It is an improved version of the AD722 and is pin-compatible when its RGB inputs are properly bypassed.

The AD724 lowers system cost, by virtue of its on-chip PLL, which enables the use of a low-cost FSC crystal for generating all the timing. However, it will also accept FSC or 4FSC clocks, and it can accept CSYNC or HSYNC/VSYNC. It uses a single +5-V supply, is packaged in a 16-pin SOIC for operation from 0 to +70°C. Price (1000s) is $4.55, and less than $3 in 10,000s.

Faxcode* 2056 or Circle 28

Pulsewidth Modulator

AD9561: for high-resolution copier- & printer applications

The AD9561 is a second-generation high-speed, digitally programmable pulsewidth modulator (PWM). Its output pulsewidth is proportional to an 8-bit digital word (from 5 ns to 100% FS). Two additional control inputs determine if the pulse is located at the beginning, middle, or end of the clock period. Pulsewidth and placement can be changed every clock cycle up to 60 MHz.

It is principally useful in copiers and printers that feature very high resolution and/or image quality ("photorealistic" is the appropriate buzzword). Pulse modulation is the only cost-effective method to obtain both high spatial resolution and wide gray-scale dynamic range (see *Analog Dialogue* 27-2, pp. 10-11). The AD9561 operates from a +5-V supply and is housed in a 28-lead SOIC. It operates over the 0 to +70°C temperature range. Price in 1000s is $7.40.

Faxcode* 2027 or Circle 29

155-Mbps Transceiver

AD6816: A complete ATM chip for UTP#5 copper or fiber

The AD6816 provides a single-chip physical layer solution for interfacing an asynchronous transfer-mode (ATM) user-network interface IC to either a Category #5 unshielded twisted pair (UTP) system or a fiber optic system. The AD6816 provides line equalization and baseline restoration, line driver, clock recovery and data retiming, local reference clock oscillator, and frequency synthesis functions. Typical applications are in network interface cards and switching-hub multiport boards.

Complying with ATM UNI 3.1 and SONET/SDH OC-3/STM1, it offers a lowest power, complete solution for analog functions, and allows partitioning between analog and digital functions for a lowest-cost system solution. It is housed in a TQFP-44 for 0 to +70°C and +5-V supply (95 mA max). Price (10,000s) is $23.45.

Faxcode* 2080 or Circle 30

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Ask The Applications Engineer—24

by Steve Guinta

RESISTANCE

Q. I'd like to understand the differences between available resistor types and how to select the right one for a particular application.

A. Sure, let's talk first about the familiar "discrete" or axial-lead type resistors we're used to working with in the lab; then we'll compare cost and performance tradeoffs of the discretes and thin- or thick-film networks.

Axial Lead Types: The three most common types of axial-lead resistors we'll talk about are *carbon composition*, or carbon film, *metal film* and *wirewound*:

- *carbon composition* or carbon film-type resistors are used in general-purpose circuits where initial accuracy and stability with variations of temperature aren't deemed critical. Typical applications include their use as a collector or emitter load, in transistor/FET biasing networks, as a discharge path for charged capacitors, and as pull-up and/or pull-down elements in digital logic circuits.

Carbon-type resistors are assigned a series of standard values (Table 1) in a quasi-logarithmic sequence, from 1 ohm to 22 megohms, with tolerances from 2% (carbon film) to 5% up to 20% (carbon composition). Power dissipation ratings range from 1/8 watt up to 2 watts. The 1/4-watt and 1/2-watt, 5% and 10% types tend to be the most popular.

Carbon-type resistors have a poor temperature coefficient (typically 5,000 ppm/°C); so they are not well suited for precision applications requiring little resistance change over temperature, but they are inexpensive—as little as 3 cents [USD 0.03] each in 1,000 quantities.

Table 1 lists a decade (10:1 range) of standard resistance values for 2% and 5% tolerances, spaced 10% apart. The smaller subset in lightface denote the only values available with 10% or 20% tolerances; they are spaced 20% apart.

Table 1. Standard resistor values: 2%, 5% and 10%

10	**16**	27	**43**	68
11	18	**30**	47	**75**
12	**20**	33	**51**	82
13	22	**36**	56	**91**
15	**24**	39	**62**	100

Carbon-type resistors use color-coded bands to identify the resistor's ohmic value and tolerance:

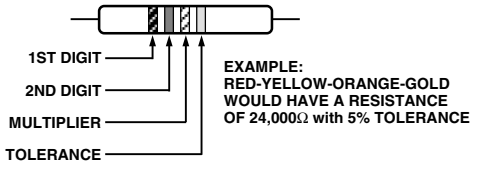


Table 2. Color code for carbon-type resistors

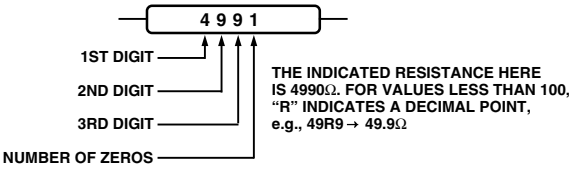
digit	color	multiple	# of zeros	tolerance
–	silver	0.01	–2	10%
–	gold	0.10	–1	5%
0	black	1	0	–
1	brown	10	1	–
2	red	100	2	2%
3	orange	1 k	3	–
4	yellow	10 k	4	–
5	green	100 k	5	–
6	blue	1 M	6	–
7	violet	10 M	7	–
8	gray	–	–	–
9	white	–	–	–
–	none	–	–	20%

- *Metal film* resistors are chosen for precision applications where initial accuracy, low temperature coefficient, and lower noise are required. Metal film resistors are generally composed of Nichrome, tin oxide or tantalum nitride, and are available in either a hermetically sealed or molded phenolic body. Typical applications include bridge circuits, RC oscillators and active filters. Initial accuracies range from 0.1 to 1.0 %, with temperature coefficients ranging between 10 and 100 ppm/°C. Standard values range from 10.0 Ω to 301 kΩ in discrete increments of 2% (for 0.5% and 1% rated tolerances).

Table 3. Standard values for film-type resistors

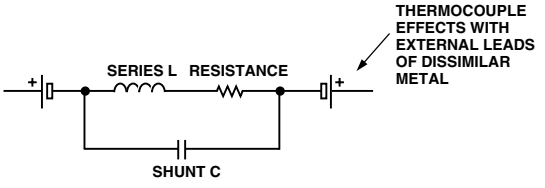
1.00	1.29	1.68	2.17	2.81	3.64	4.70	6.08	7.87
1.02	1.32	1.71	2.22	2.87	3.71	4.80	6.21	8.03
1.04	1.35	1.74	2.26	2.92	3.78	4.89	6.33	8.19
1.06	1.37	1.78	2.31	2.98	3.86	4.99	6.46	8.35
1.08	1.40	1.82	2.35	3.04	3.94	5.09	6.59	8.52
1.10	1.43	1.85	2.40	3.10	4.01	5.19	6.72	8.69
1.13	1.46	1.89	2.45	3.17	4.09	5.30	6.85	8.86
1.15	1.49	1.93	2.50	3.23	4.18	5.40	6.99	9.04
1.17	1.52	1.96	2.55	3.29	4.26	5.51	7.13	9.22
1.20	1.55	2.00	2.60	3.36	4.34	5.62	7.27	9.41
1.22	1.58	2.04	2.65	3.43	4.43	5.73	7.42	9.59
1.24	1.61	2.09	2.70	3.49	4.52	5.85	7.56	9.79
1.27	1.64	2.13	2.76	3.56	4.61	5.96	7.72	9.98

Metal film resistors use a 4 digit numbering sequence to identify the resistor value instead of the color band scheme used for carbon types:



• *Wirewound* precision resistors are extremely accurate and stable (0.05%, <10 ppm/°C); they are used in demanding applications, such as tuning networks and precision attenuator circuits. Typical resistance values run from 0.1 Ω to 1.2 MΩ.

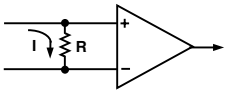
High Frequency Effects: Unlike its "ideal" counterpart, a "real" resistor, like a real capacitor (*Analog Dialogue* 30-2), suffers from parasitics. (Actually, any two-terminal element may look like a resistor, capacitor, inductor, or damped resonant circuit, depending on the frequency it's tested at.)



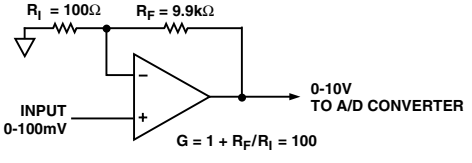
Factors such as resistor base material and the ratio of length to cross-sectional area determine the extent to which the parasitic L and C affect the constancy of a resistor's effective dc resistance at high frequencies. Film type resistors generally have excellent high-frequency response; the best maintain their accuracy to about 100 MHz. Carbon types are useful to about 1 MHz. Wirewound resistors have the highest inductance, and hence the poorest frequency response. Even if they are non-inductively wound, they tend to have high capacitance and are likely to be unsuitable for use above 50 kHz.

Q. What about temperature effects? Should I always use resistors with the lowest temperature coefficients (TCRs)?

A. Not necessarily. A lot depends on the application. For the single resistor shown here, measuring current in a loop, the current produces a voltage across the resistor equal to I × R. In this application, the absolute accuracy of resistance at any temperature would be critical to the accuracy of the current measurement, so a resistor with a very low TC would be used.



A different example is the behavior of gain-setting resistors in a gain-of-100 op amp circuit, shown below. In this type of application, where gain accuracy depends on the ratio of resistances (a ratiometric configuration), resistance matching, and the tracking of the resistance temperature coefficients (TCRs), is more critical than absolute accuracy.



Here are a couple of examples that make the point.

1. Assume both resistors have an actual TC of 100 ppm/°C (i.e., 0.01%/°C). The resistance following a temperature change, ΔT, is

$$R = R_0(1+ TC\,\Delta T)$$

For a 10°C temperature rise, both R_f and R_i increase by 0.01%/°C × 10°C = 0.1%. Op amp gains are [to a very good approximation] $1 + R_F/R_I$. Since both resistance values, though quite different (99:1), have increased by the same *percentage*, their ratio—hence the gain—is unchanged. Note that the gain accuracy depends just on the resistance *ratio*, independently of the absolute values.

2. Assume that R_I has a TC of 100 ppm/°C, but R_F's TC is only 75 ppm/°C. For a 10°C change, R_I increases by 0.1% to 1.001 times its initial value, and R_F increases by 0.075% to 1.00075 times its initial value. The new value of gain is

$$(1.00075\ R_F)/(1.001\ R_I) = 0.99975\ R_F/R_I$$

For an ambient temperature change of 10°C, the amplifier circuit's gain has decreased by 0.025% (equivalent to 1 LSB in a 12-bit system).

Another parameter that's not often understood is the self-heating effect in a resistor.

Q. What's that?

A. Self-heating causes a change in resistance because of the increase in temperature when the dissipated power increases. Most manufacturers' data sheets will include a specification called "thermal resistance" or "thermal derating", expressed in degrees C per watt (°C/W). For a 1/4-watt resistor of typical size, the thermal resistance is about 125°C/W. Let's apply this to the example of the above op amp circuit for full-scale input:

Power dissipated by R_I is

E^2/R = (100 mV)^2/100 Ω = 100 μW, leading to a temperature change of 100 μW × 125°C/W = 0.0125°C, and a negligible 1-ppm resistance change (0.00012%).

Power dissipated by R_F is

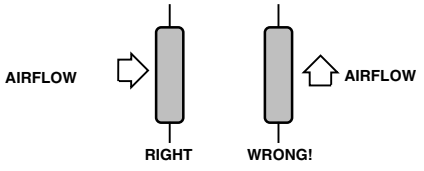
$^2/R$ = (9.9 V)^2/9900 Ω = 9.9 mW, leading to a temperature change of 0.0099 W × 125°C/W = 1.24°C, and a resistance change of 0.0124%, which translates directly into a 0.012% gain change.

Thermocouple Effects: Wirewound precision resistors have another problem. The junction of the resistance wire and the resistor lead forms a thermocouple which has a thermoelectric EMF of 42 μV/°C for the standard "Alloy 180"/Nichrome junction of an ordinary wirewound resistor. If a resistor is chosen with the [more expensive] copper/nichrome junction, the value is 2.5 μV/°C. ("Alloy 180" is the standard component lead alloy of 77% copper and 23% nickel.)

Such thermocouple effects are unimportant in ac applications, and they cancel out when both ends of the resistor are at the same temperature; however if one end is warmer than the other, either because of the power being dissipated in the resistor, or

its location with respect to heat sources, the net thermoelectric EMF will introduce an erroneous dc voltage into the circuit. With an ordinary wirewound resistor, a temperature differential of only 4°C will introduce a dc error of 168 μV—which is greater than 1 LSB in a 10-V/16-bit system!

This problem can be fixed by mounting wirewound resistors so as to insure that temperature differentials are minimized. This may be done by keeping both leads of equal length, to equalize thermal conduction through them, by insuring that any airflow (whether forced or natural convection) is normal to the resistor body, and by taking care that both ends of the resistor are at the same thermal distance (i.e., receive equal heat flow) from any heat source on the PC board.



Q. What are the differences between "thin-film" and "thick-film" networks, and what are the advantages/disadvantages of using a resistor network over discrete parts?

A. Besides the obvious advantage of taking up considerably less real estate, resistor networks—whether as a separate entity, or part of a monolithic IC—offer the advantages of high accuracy via laser trimming, tight TC matching, and good temperature tracking. Typical applications for discrete networks are in precision attenuators and gain setting stages. Thin film networks are also used in the design of monolithic (IC) and hybrid instrumentation amplifiers, and in CMOS D/A and A/D converters that employ an R-2R Ladder network topology.

Thick film resistors are the lowest-cost type—they have fair matching (<0.1%), but poor TC performance (>100 ppm/°C) and tracking (>10 ppm/°C). They are produced by screening or electroplating the resistive element onto a substrate material, such as glass or ceramic.

Thin film networks are moderately priced and offer good matching (0.01%), plus good TC (<100 ppm/°C) and tracking (<10 ppm/°C). All are laser trimmable. Thin film networks are manufactured using vapor deposition.

Tables 4 compares the advantages/disadvantages of a thick film and several types of thin-film resistor networks. Table 5 compares substrate materials.

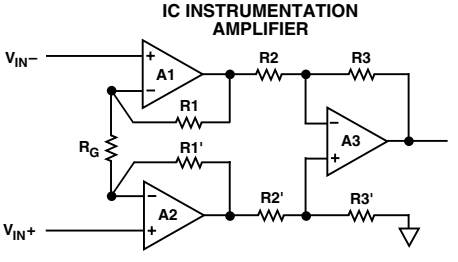
Table 4. Resistor Networks

Type	Advantages	Disadvantages
Thick film	Low cost	Fair matching (0.1%)
	High power	Poor TC (>100 ppm/°C)
	Laser-trimmable	Poor tracking TC
	Readily available	(10 ppm/°C)
Thin film on glass	Good matching (<0.01%)	Delicate
	Good TC (<100 ppm/°C)	Often large geometry
	Good tracking TC (2 ppm/°C)	Low power
	Moderate cost	
	Laser-trimmable	
	Low capacitance	
Thin film on ceramic	Good matching (<0.01%)	Often large geometry
	Good TC (<100 ppm/°C)	
	Good tracking TC (2 ppm/°C)	
	Moderate cost	
	Laser-trimmable	
	Low capacitance	
	Suitable for hybrid IC substrate	
Thin film on silicon	Good matching (<0.01%)	
	Good TC (<100 ppm/°C)	
	Good tracking TC (2 ppm/°C)	
	Moderate cost	
	Laser-trimmable	
	Low capacitance	
	Suitable for hybrid IC substrate	

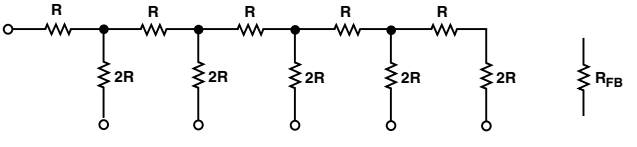
Table 5. Substrate Materials

Substrate	Advantages	Disadvantages
Glass	Low capacitance	Delicate
		Low power
		Large geometry
Ceramic	Low capacitance	Large geometry
	Suitable for hybrid IC substrate	
Silicon	Suitable for monolithic construction	Low power
		Capacitance to substrate
Sapphire	Low capacitance	Low power
		Higher cost

In the example of the IC instrumentation amplifier shown below, tight matching between resistors R1-R1', R2-R2', R3-R3' insures high common-mode rejection (as much as 120 dB, dc to 60 Hz). While it is possible to achieve higher common-mode rejection using discrete op amps and resistors, the arduous task of matching the resistor elements is undesirable in a production environment.



Matching, rather than absolute accuracy, is also important in R-2R ladder networks (including the feedback resistor) of the type used in CMOS D/A converters. To achieve *n*-bit performance, the resistors have to be matched to within 1/2*n*, which is easily achieved through laser trimming. Absolute accuracy error, however, can be as much as ±20%. Shown here is a typical R-2R ladder network used in a CMOS digital-analog converter.



Worth Reading

SERIALS

COMMUNICATIONS DIRECT—Systems and IC solutions for demanding markets: Volume 2, No. 2 (December, 1996, 8 pages). Features articles on Broadband, low-cost ADSL chipset, cable modems. And more . . . **FREE, Circle 31**

APPLICATION NOTES

Amplitude modulation of the AD9850 Direct Digital Synthesizer, by Richard Cushing [2 pp., AN-423]. **Circle 32**

High-speed data acquisition using the RTI®-2100 Series, by Jim Maxwell [8 pp., AN-421]. **Circle 33**

NEW DATA SHEETS

AD8400/AD8402/AD8403 1-/2-/4-channel digital potentiometers. **Circle 34**

AD73311 Low-cost, low-power CMOS general-purpose analog front end. [Codec for consumer and telephony applications includes 16-bit A/D and 16-bit D/A channels.] **Circle 35**

ADDC02808PB 28-V, 200-W pulsed DC-DC converter with integral EMI filter. **Circle 36**

ADP1173 Micropower DC-DC converter. **Circle 37**

ADP3302 High-precision anyCAP™ dual low-dropout linear regulator. **Circle 38**

OP184/OP284/OP484 Precision rail-to-rail input & output single/dual/quad operational amplifiers. **Circle 39**

RTI-2100 Series Real-time data-acquisition system and **RTI-2100 Series Software** Software support—DOS and Windows. **Circle 40**

5B08/5B08-MUX 5B Series: 8-channel backplanes. **Circle 41**

IN THE LAST ISSUE

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For a copy, circle 42.

NEW PATENTS [*not available from Analog Devices*]

5,568,145 to David Reynolds for **MOS current source layout technique to minimize deviation** • • • 5,572,166 to Barrie Gilbert for **Linear-in-decibel variable-gain amplifier** • • • 5,574,392 to Edward Jordan for **Asymmetrical ramp generator system** • • • 5,574,454 to James Wilson and Ronald Cellini for **Digital phase-locked loop utilizing a high-order sigma-delta modulator** • • • 5,578,224 to Theresa Core for **Method of making micromachined device with ground plane under sensor** • • • 5,583,290 to Stephen Lewis for **Micromechanical apparatus with limited actuation bandwidth** • • • 5,583,713 to Peter Real, Mairtin Walsh, Kenneth Deevy, Patrick Griffin, and Philip Quinlan for **Pipelined demodulation and ADC conversion scheme for disk drive servo system** • • • 5,585,757 to Douglas Frey for **Explicit log-domain root-mean-square detector** • • • 5,587,689 to Derek Bowers for **Voltage controlled amplifier with a negative resistance circuit for reducing nonlinearity distortion** • • • 5,589,785 to Patrick J. Garavan for **Low-voltage CMOS comparator** • • • 5,589,791 to Barrie Gilbert for **Variable gain mixer having improved linearity and lower switching noise** • • • 5,589,792 to A. Paul Brokaw for **Resistor programmable temperature switch** • • • 5,591,996 to Geoffrey Haigh and Scott Munroe for **Recirculating charge transfer magnetic field sensor** • • • 5,592,120 to Wyn Palmer and Fernando Viana for **Charge pump system** • • • 5,594,266 to David Beigel, William Krieger, and Susan Feindt for **Integrated circuit (IC) with a two-terminal diode device to protect metal-oxide-metal capacitors from ESD damage.**

MORE AUTHORS *(continued from page 2)*

Jim Ryan (page 13) is a Senior Engineer with the Applications Group in Limerick, Ireland, where he provides customer support and is involved with new-product definition for CMOS converter products. He holds a BSc. in Electronic Systems and an MEng. in Computer Systems, both from the University of Limerick, and has worked previously as a designer of laboratory instrumentation. In his leisure time he enjoys rugby and hill-walking.

Albert O'Grady (page 13) is a member of the Applications Group at Analog Devices, in Limerick Ireland, in support of both analog-to-digital and digital-to-analog converter products. He holds a BEng. from the University of Limerick. In his spare time, Albert enjoys reading and plays badminton and tennis.

Dave Robertson (page 7) is a design engineer in the Analog Devices High-Speed Converter group in Wilmington, MA. His photo and a brief biography appeared in *Analog Dialogue* 30-3.

Steve Guinta (page 20) is the Technical Training Manager for ADI's Central Applications Group in Wilmington, MA. His photo and a brief biography appeared in *Analog Dialogue* 30-2.

Notice: In the last issue (*Analog Dialogue* 30-4), the article "Voltage Regulation for Power Management" (pp. 13–15) showed a circuit to maintain two regulated 3-V outputs, using a Lilon battery (Figure 2). The circuit was designed and built by **Hendrik Santos**. The ADP3000, used in that circuit, was designed by **James Ashe**; and the ADP3302 was designed by **A. Paul Brokaw** and **Giovanni Pietrobon.**—Ed.